

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

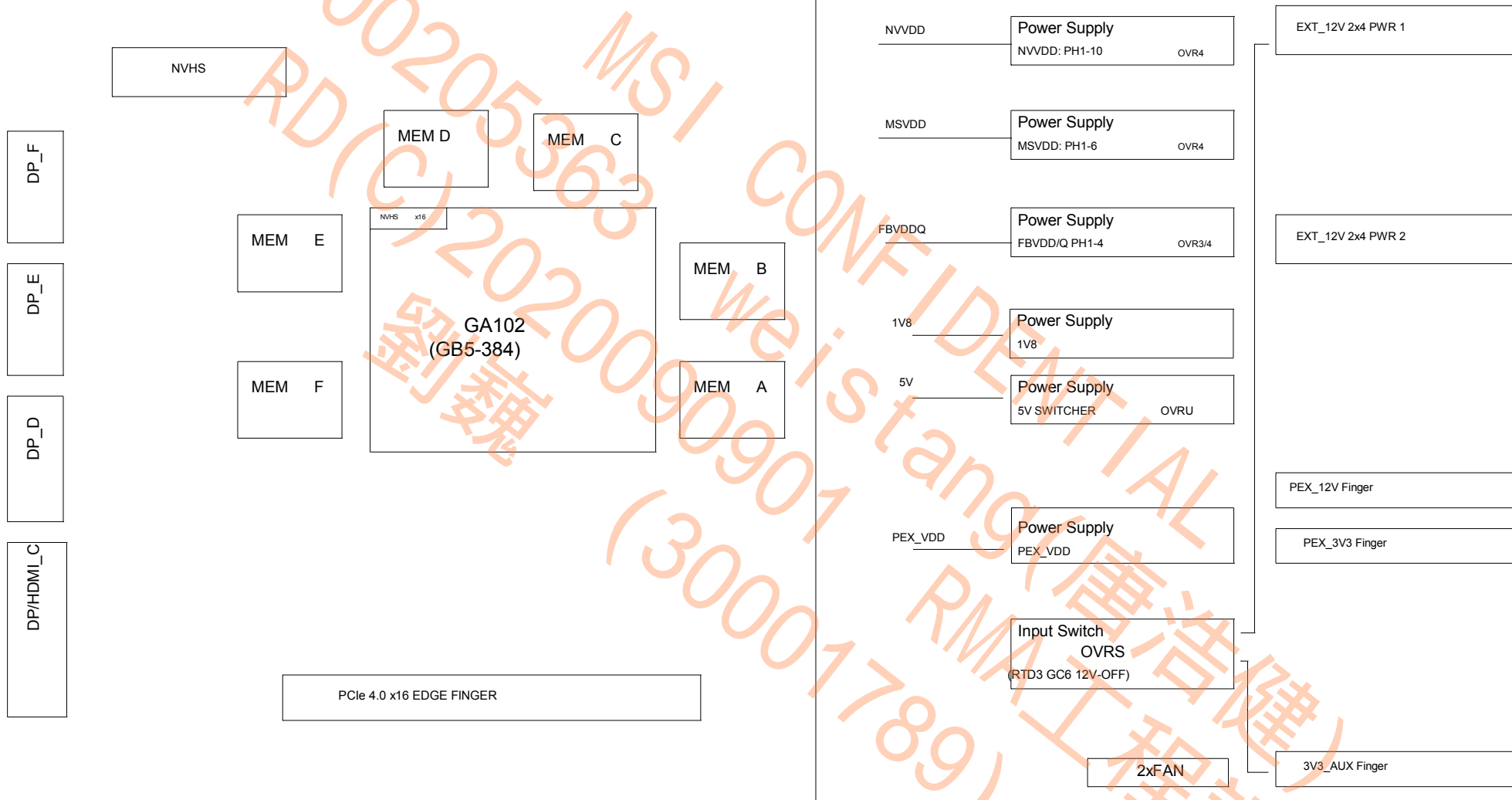
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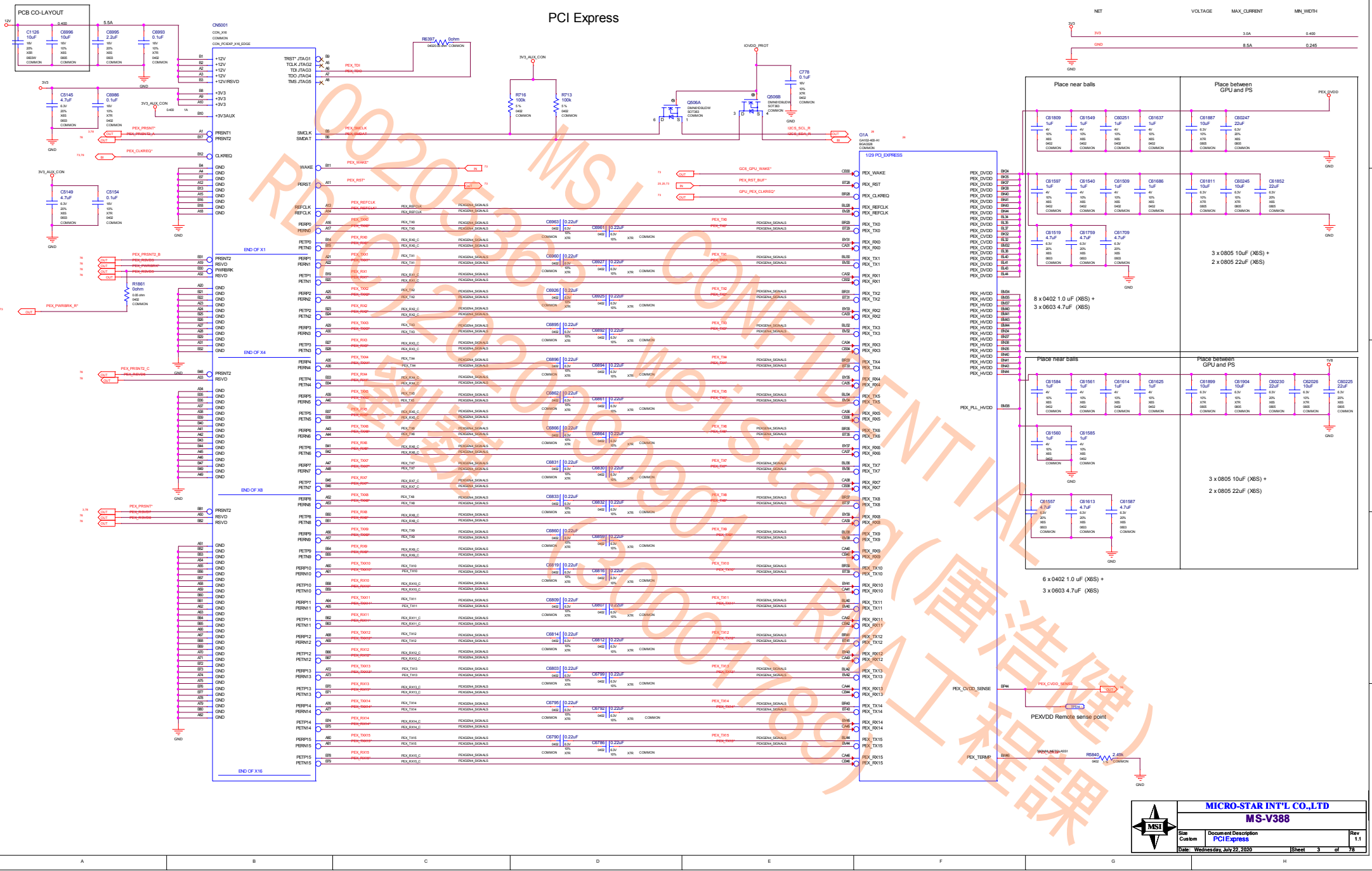
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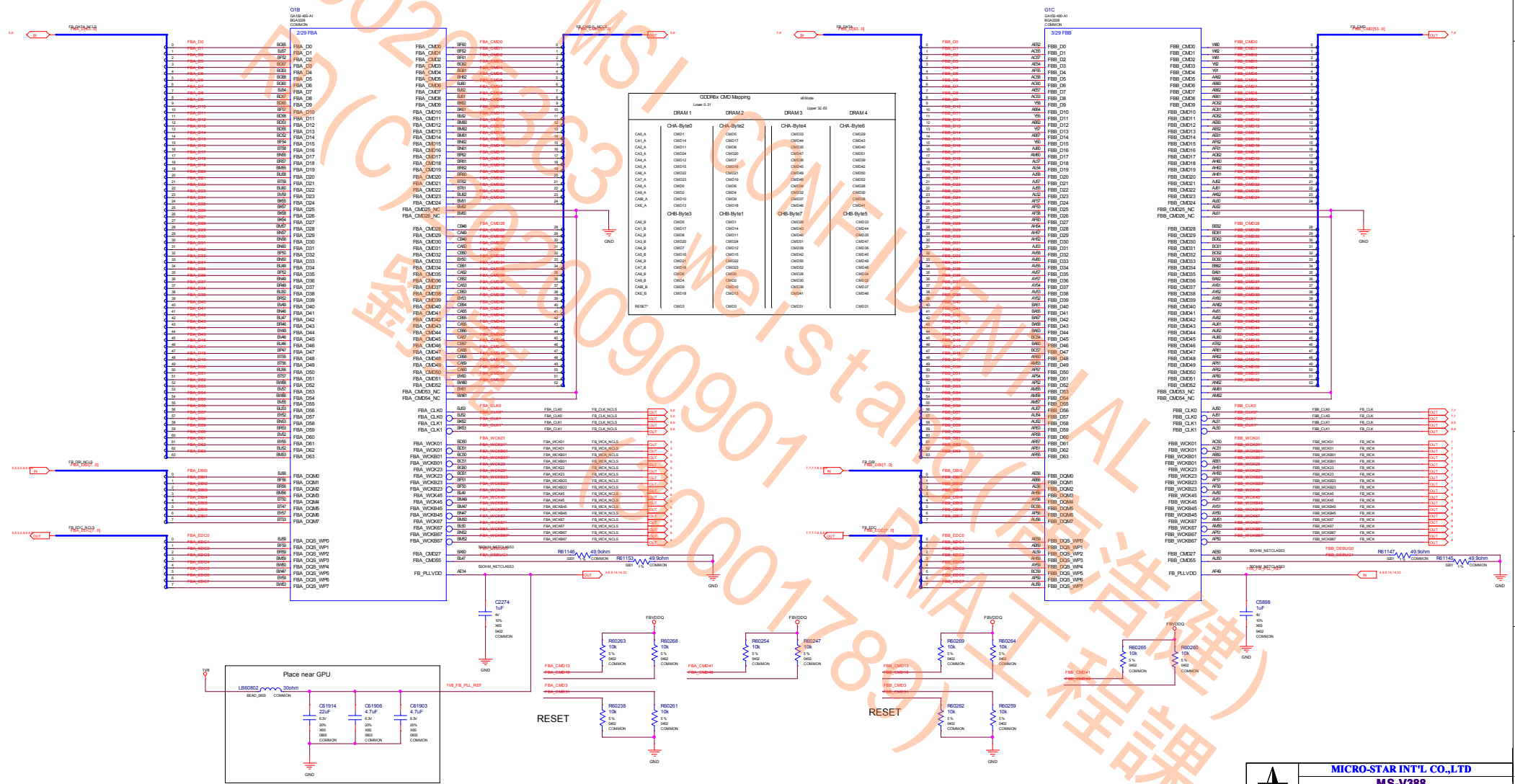
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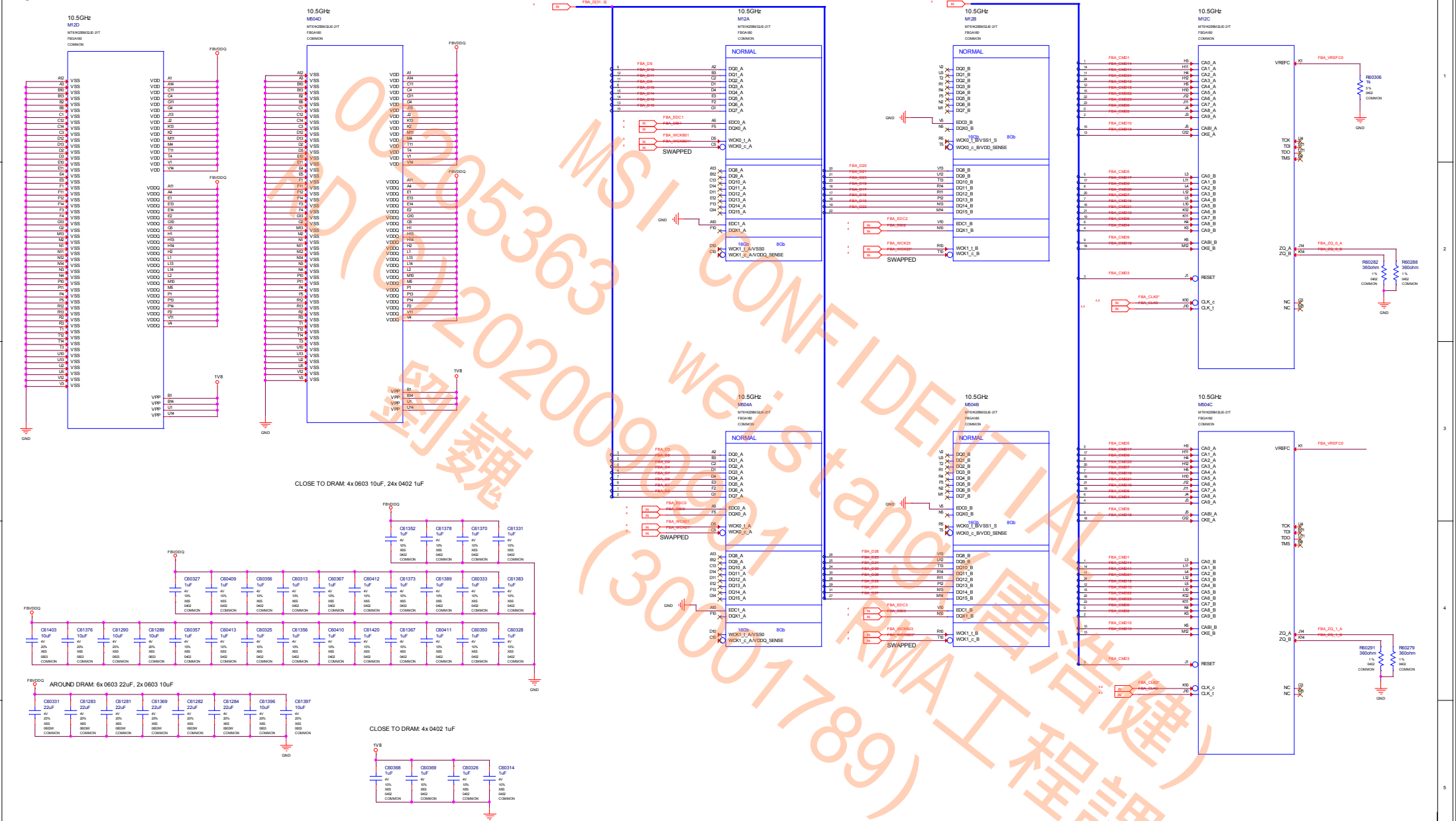
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Block Diagram







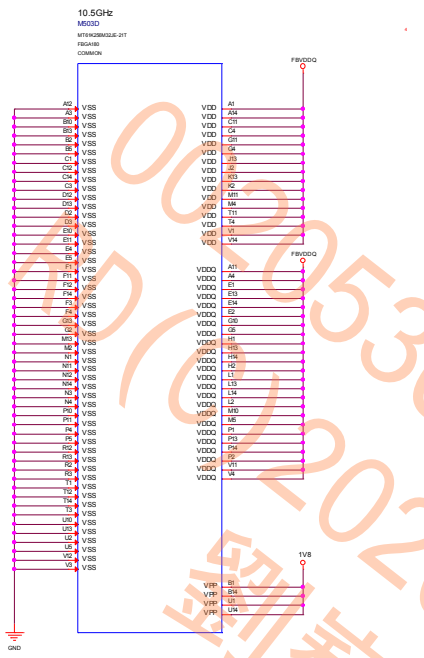




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The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It features two voltage regulators: a 5V regulator (U1) and a 3.3V regulator (U2). The 5V regulator is connected to a common ground and has a 10µF input capacitor (C1) and a 10µF output capacitor (C2). The 3.3V regulator is connected to a common ground and has a 10µF input capacitor (C3) and a 10µF output capacitor (C4). The output of the 3.3V regulator is connected to the VDDIO pin of the ADXL345 (U3). The ADXL345 is also connected to a common ground. The schematic is labeled 'FIBR02' and 'FIBR03'.

5V
GND

U1
ADP111
500mA LDO

C1
10µF

C2
10µF

5V
GND

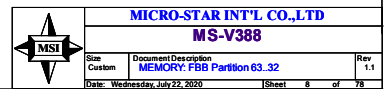
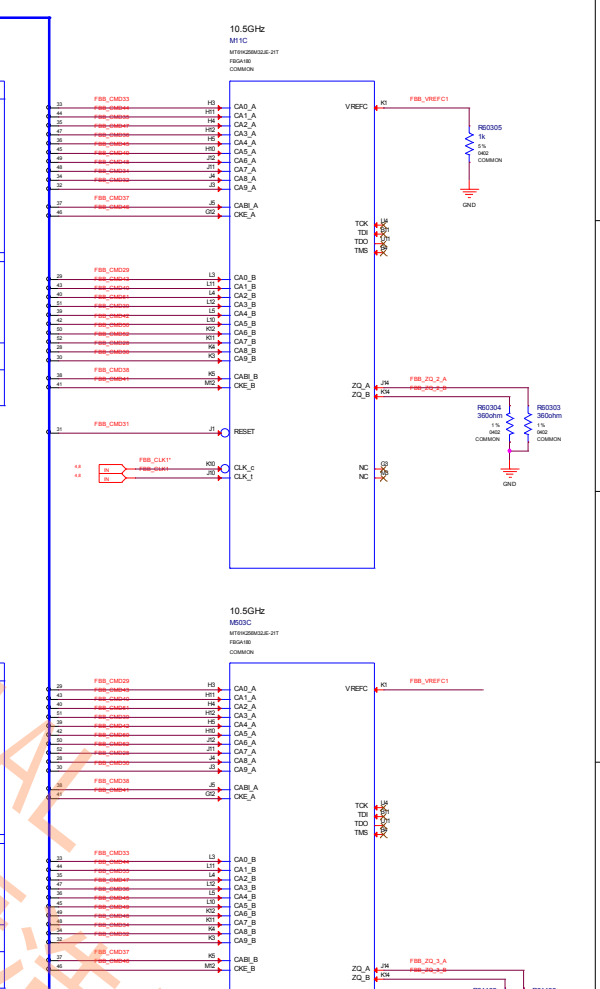
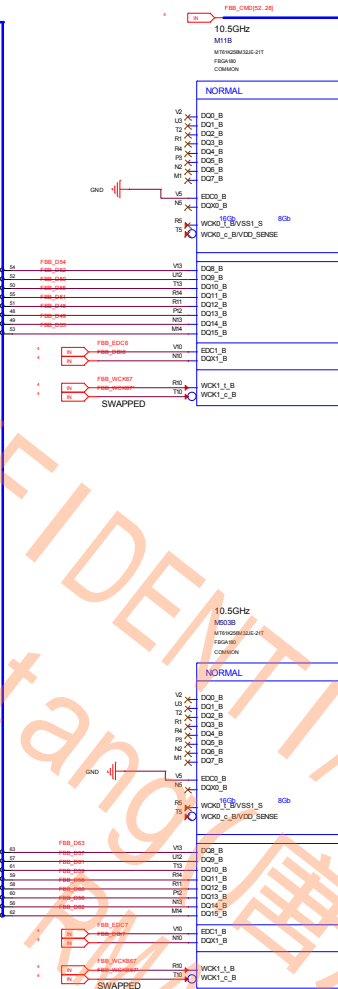
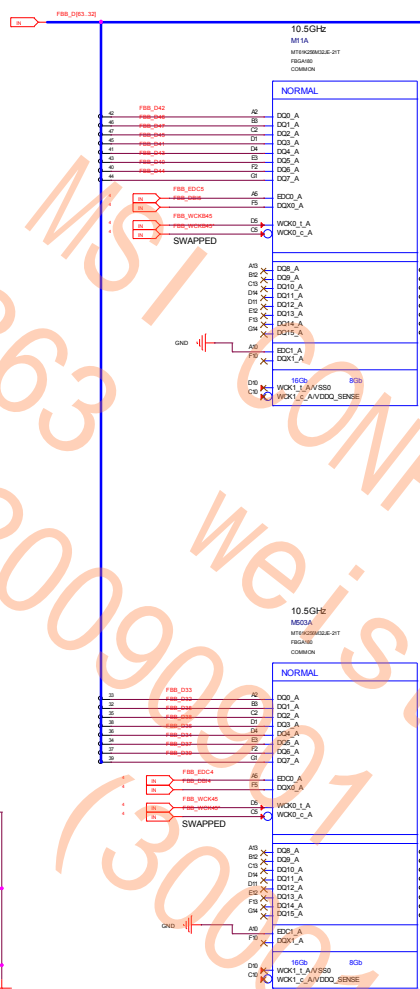
U2
ADP111
3.3V LDO

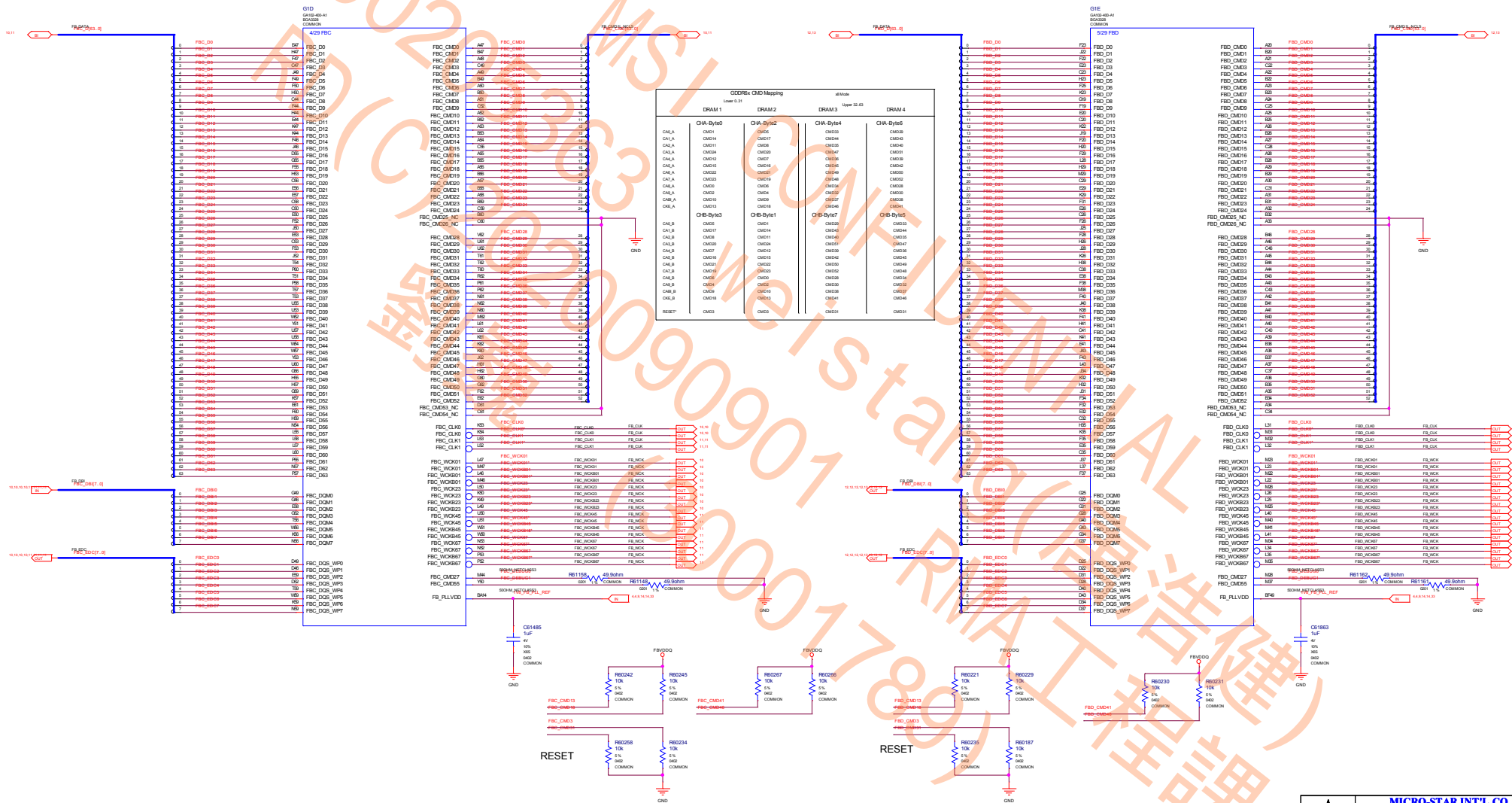
C3
10µF

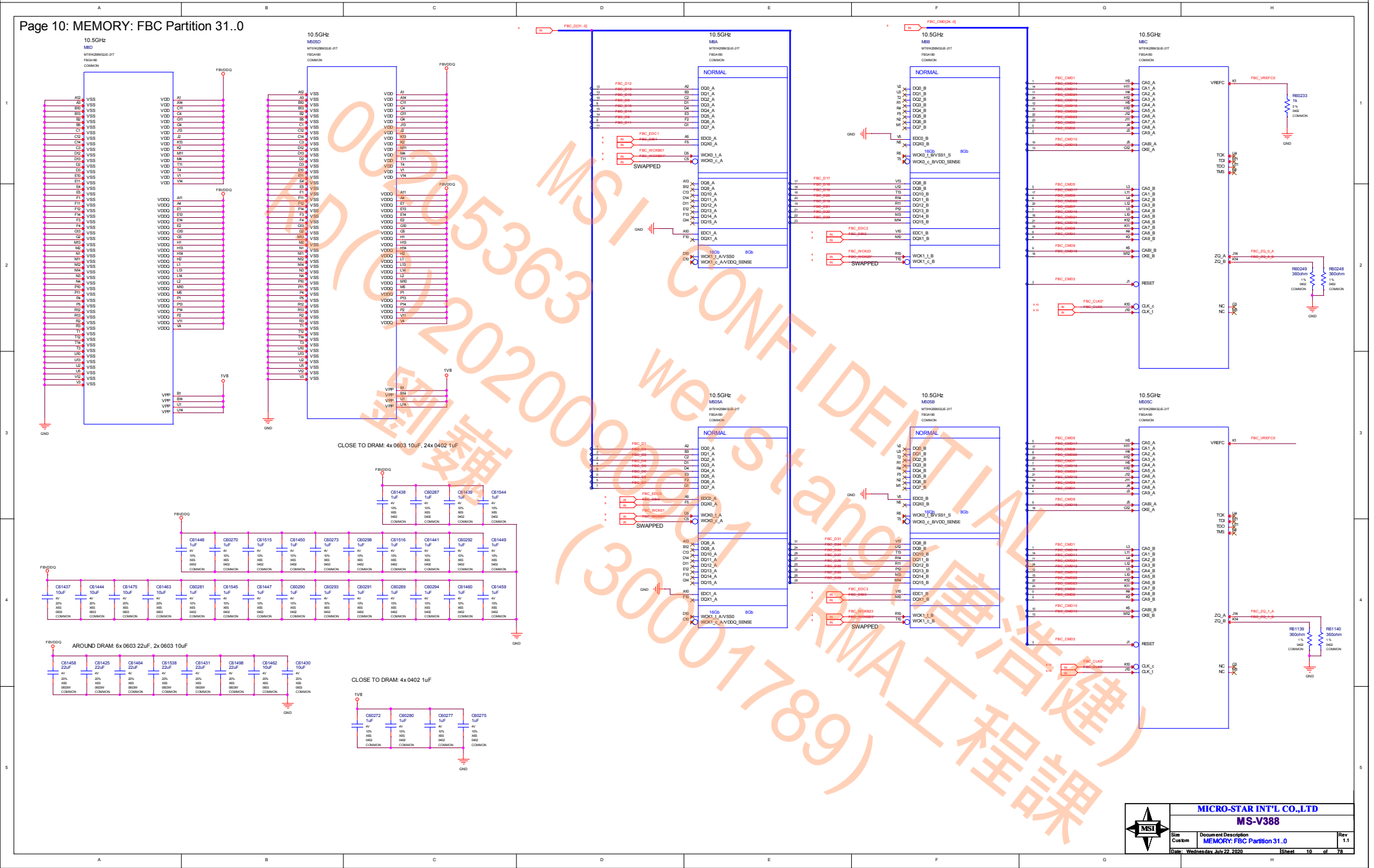
C4
10µF

3.3V
GND

CLOSE TO DRAM: 4x 0402 1uF

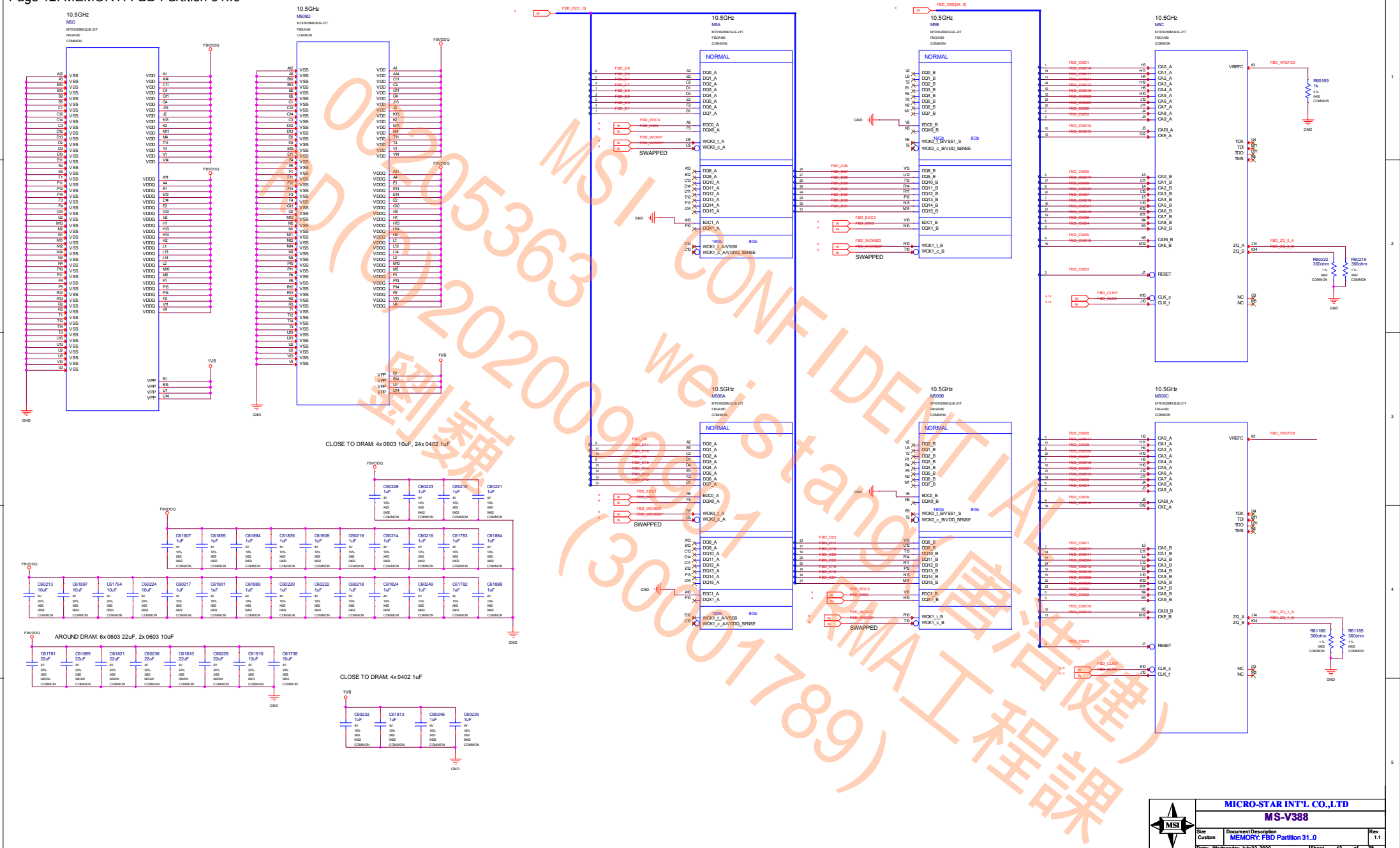


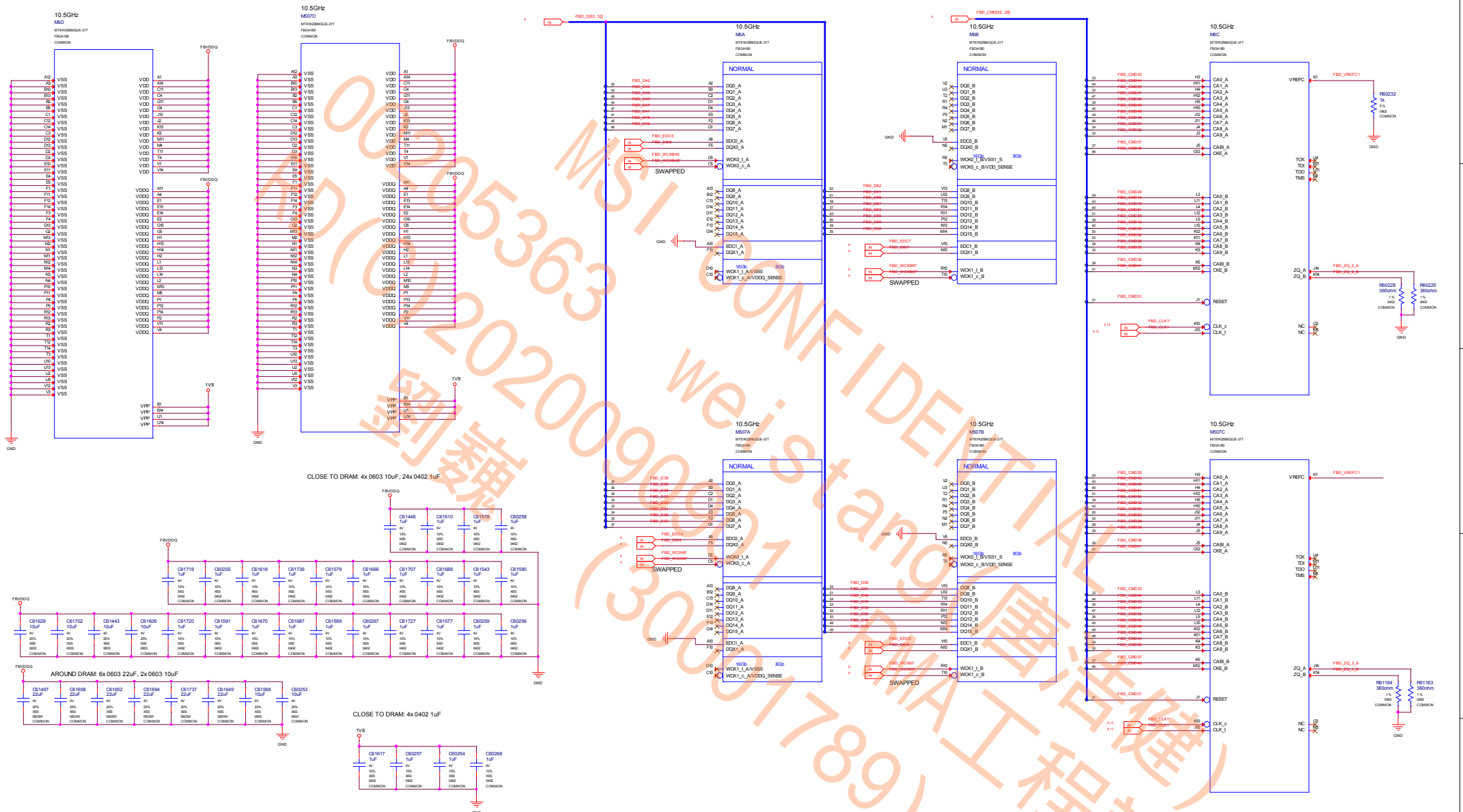


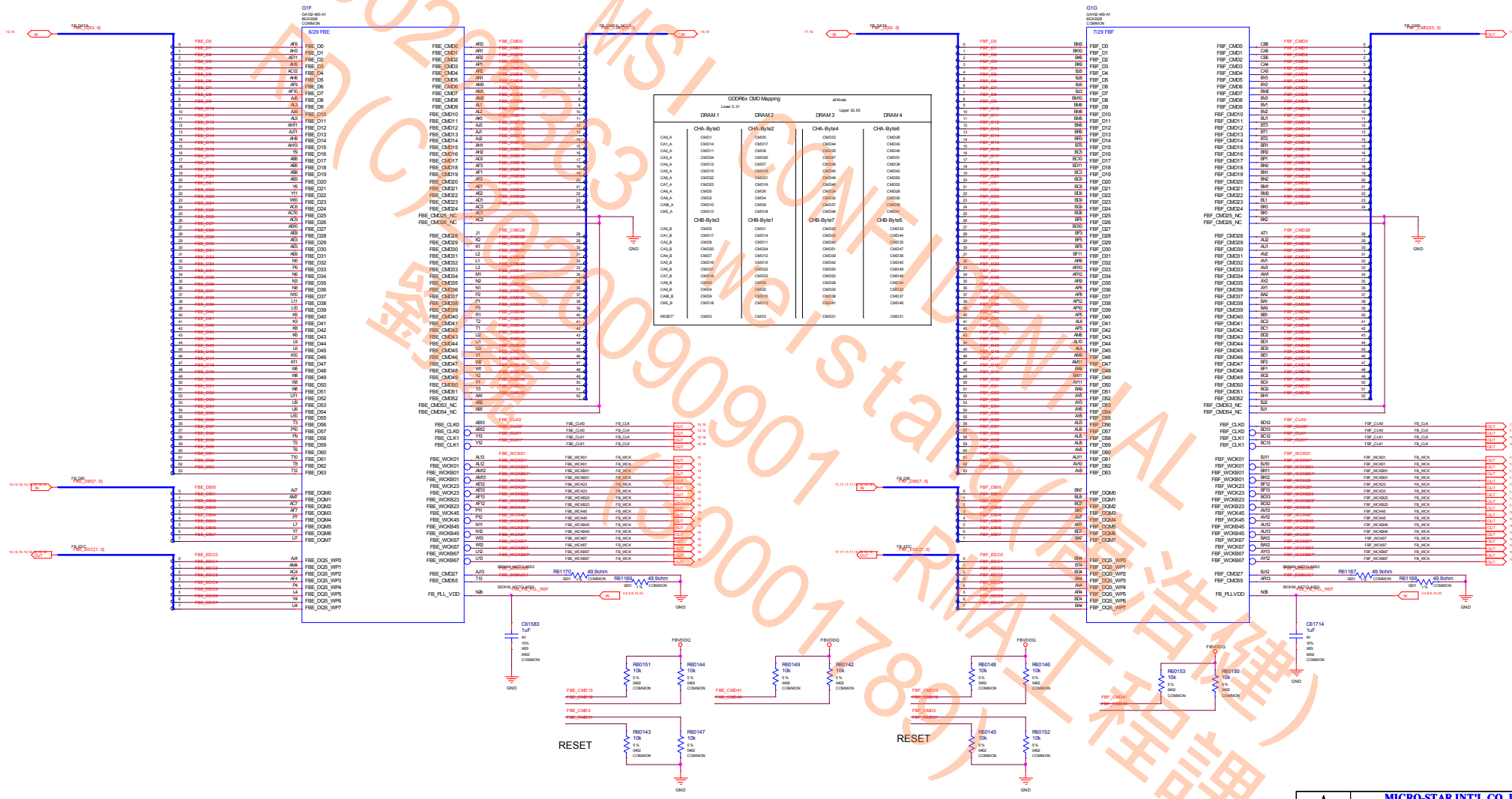


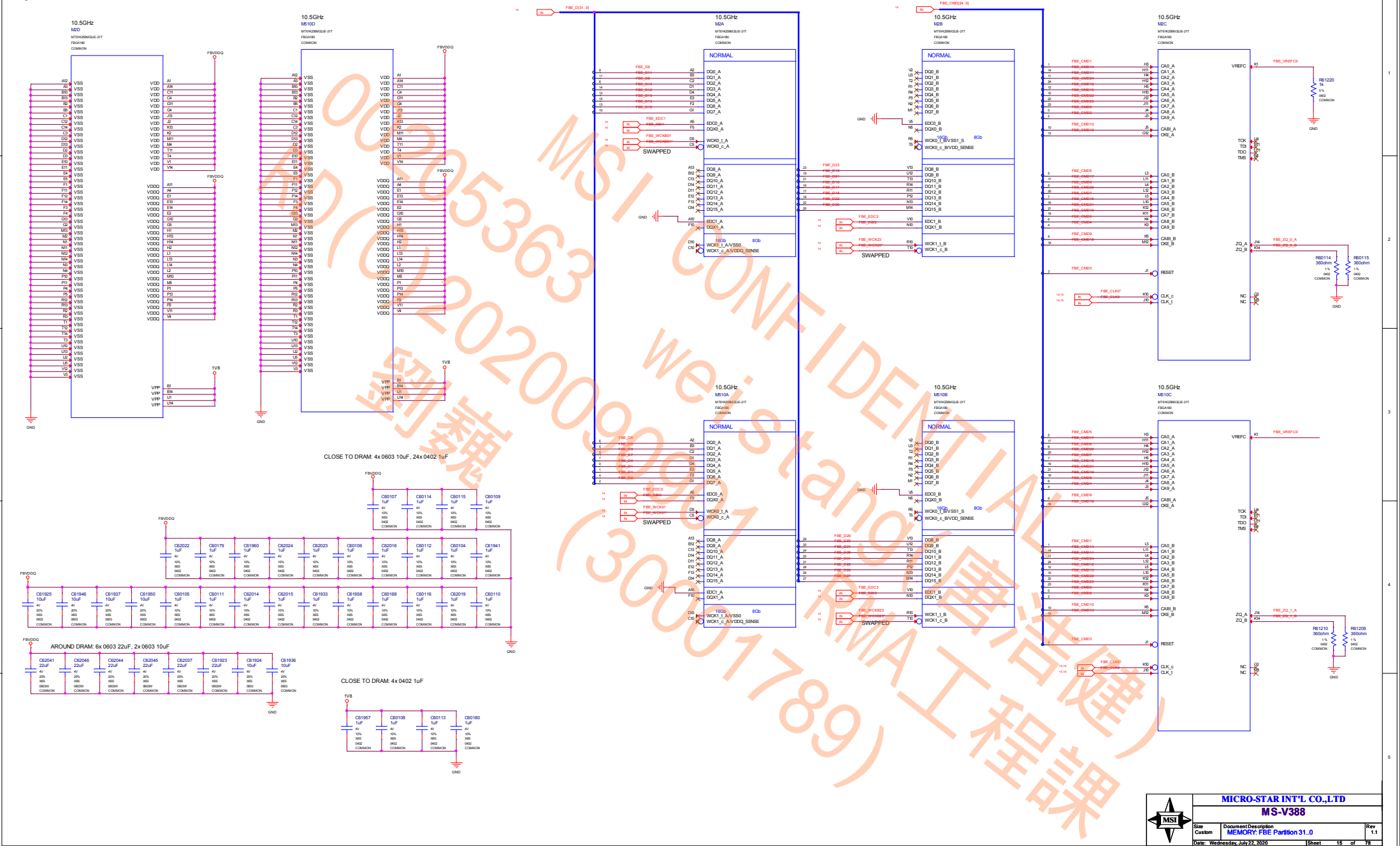
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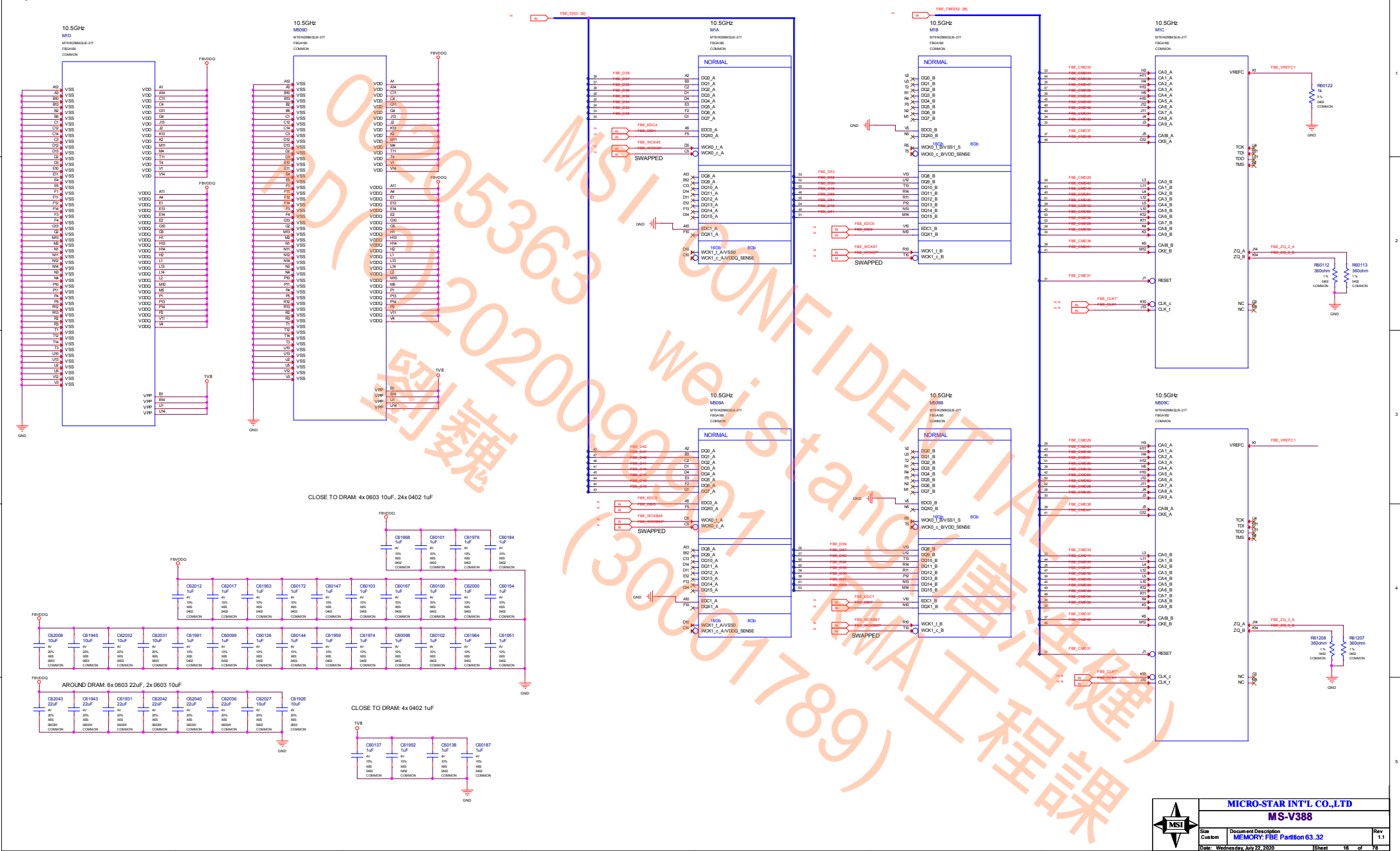
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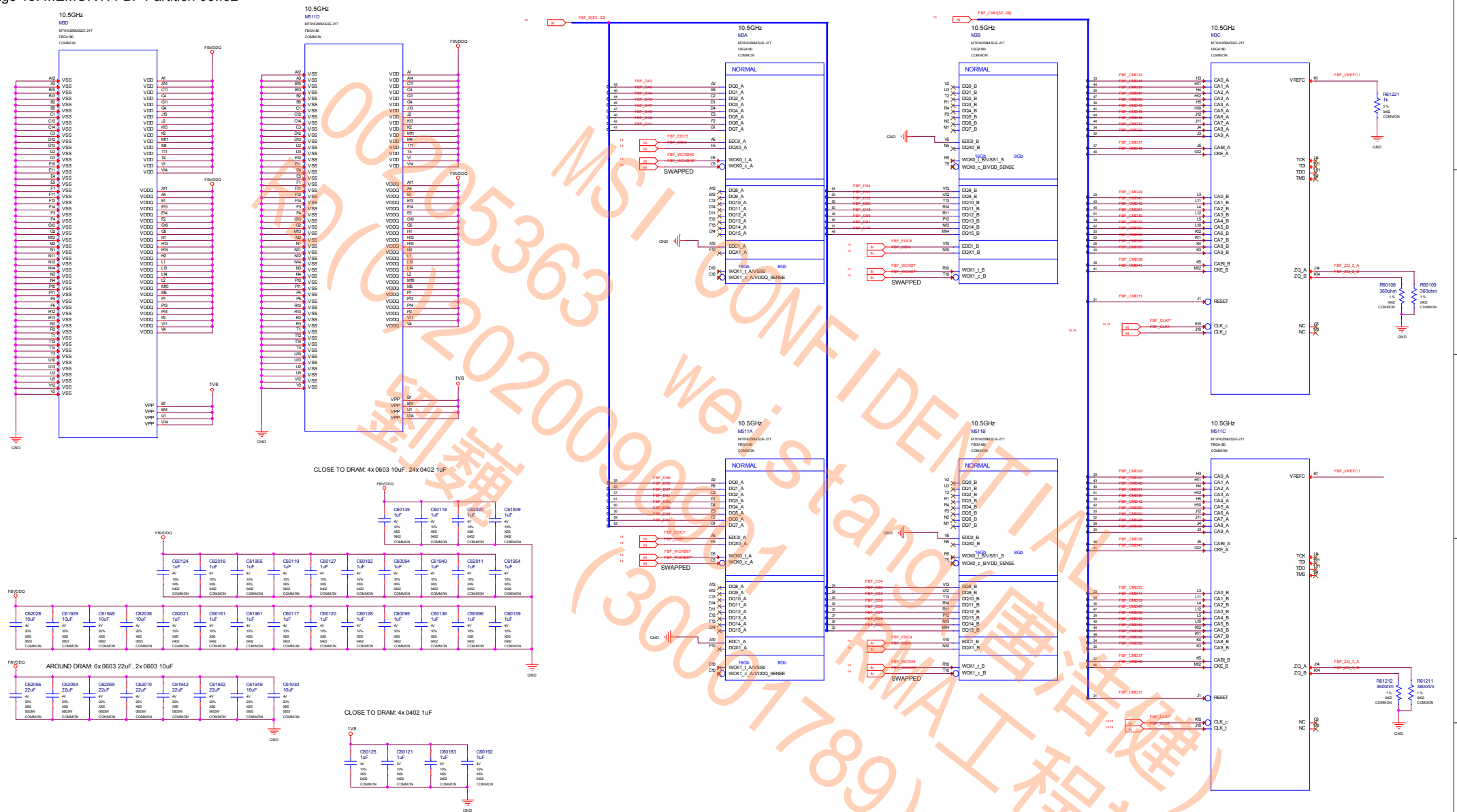












GPU GND, RFUs & RSVD

[illegible]

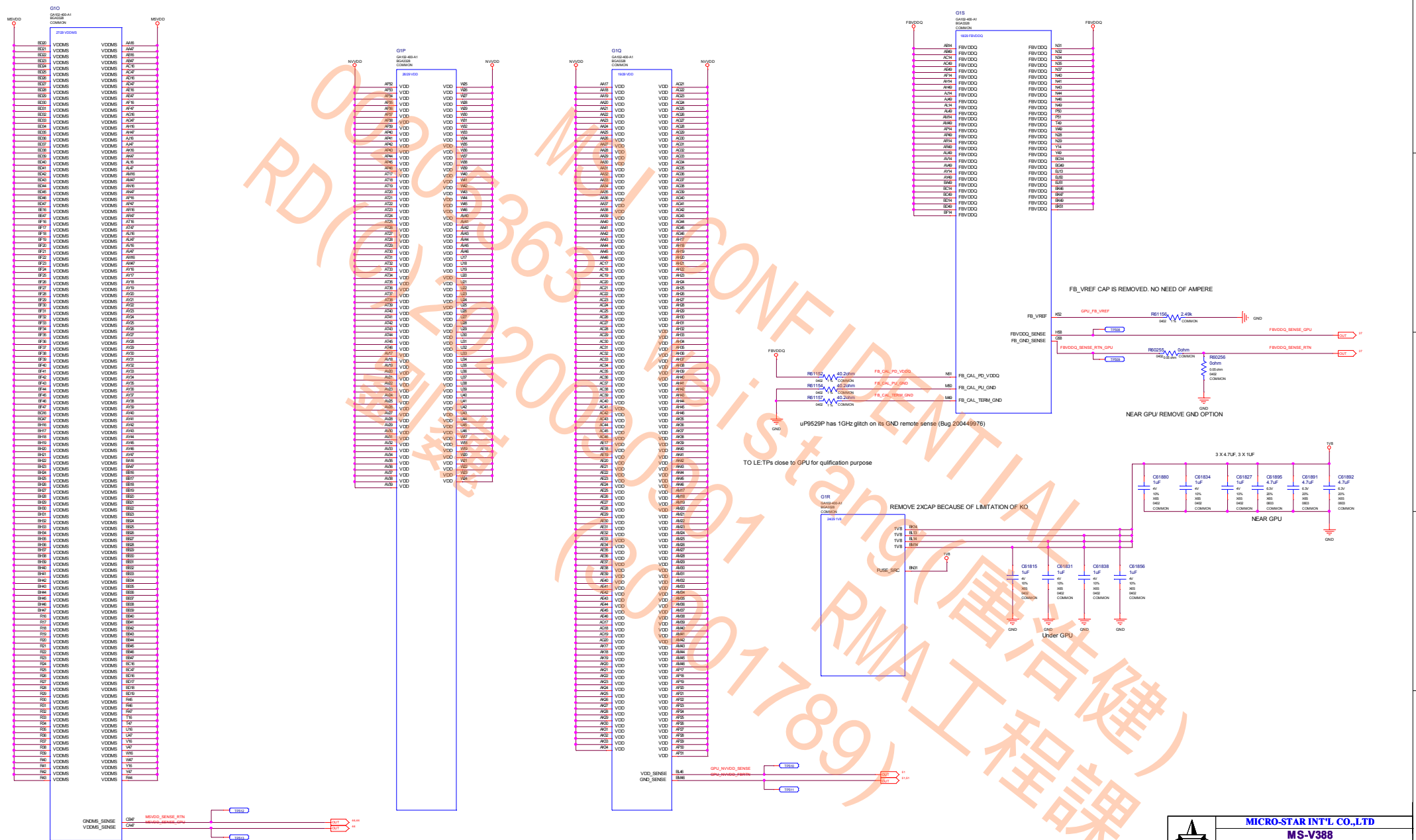
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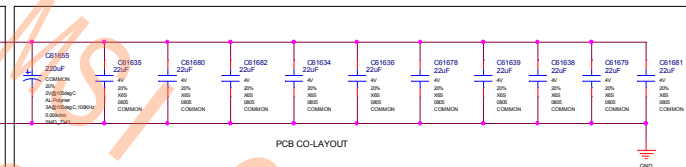
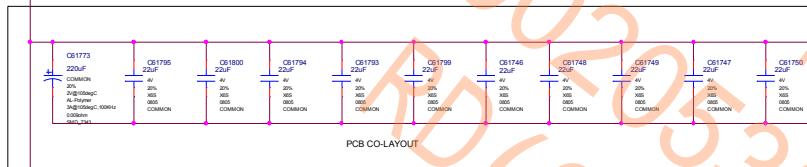
GPU PWR and GND



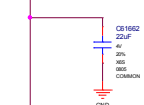
NVVDD

UNDER GPU

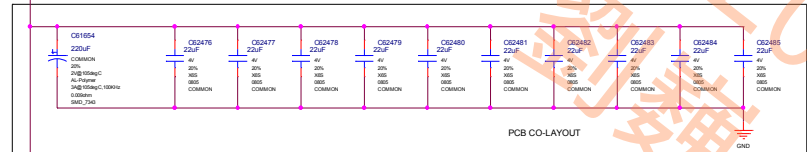
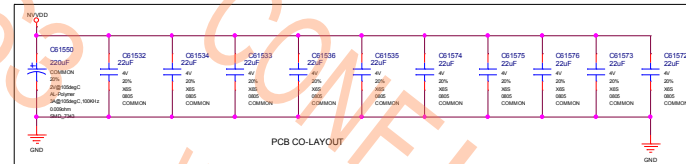
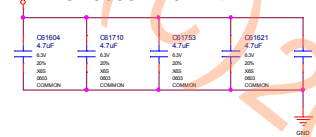
4x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 0805 22uF)



1x 0805 22uF



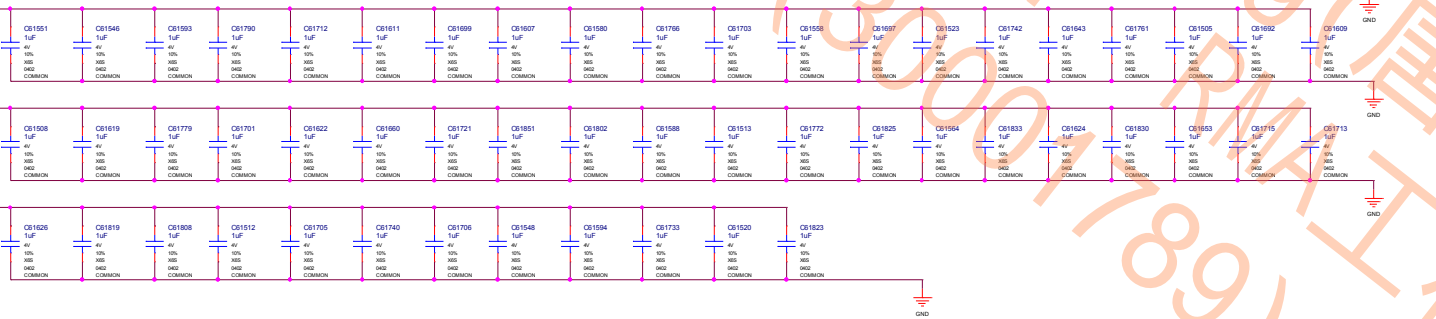
5x 0603 4.7uF



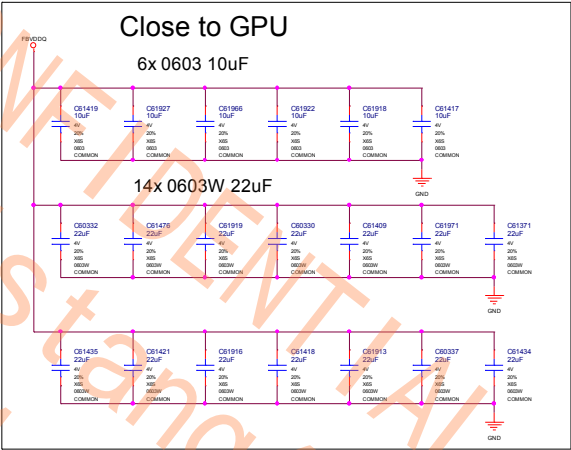
14x 0603 10uF



52 x 0402 1uF



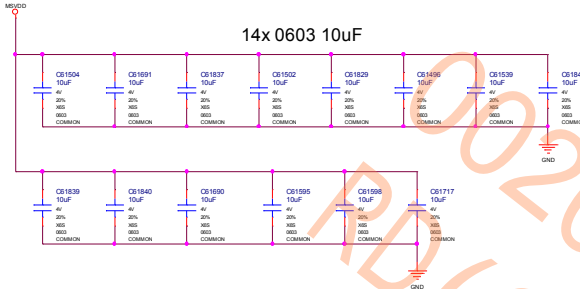
FBVDDQ



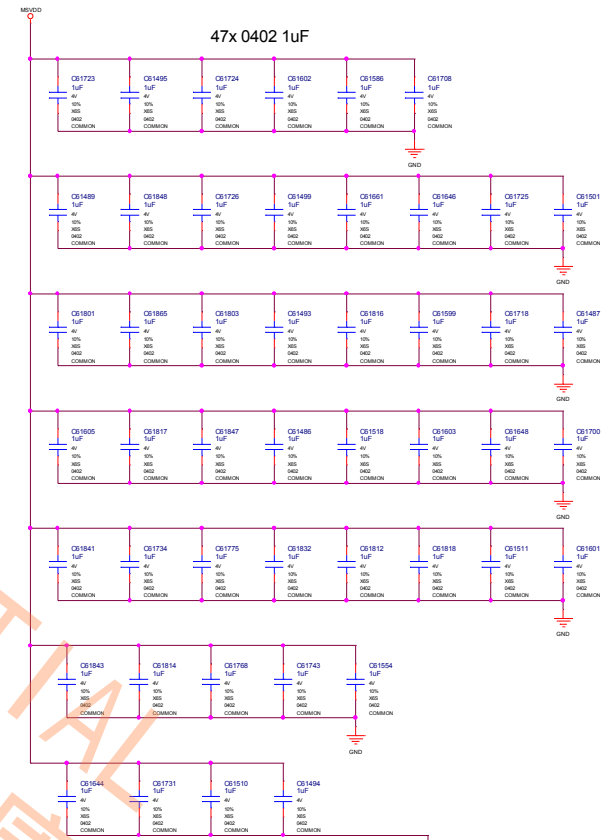
MSVDD

UNDER GPU

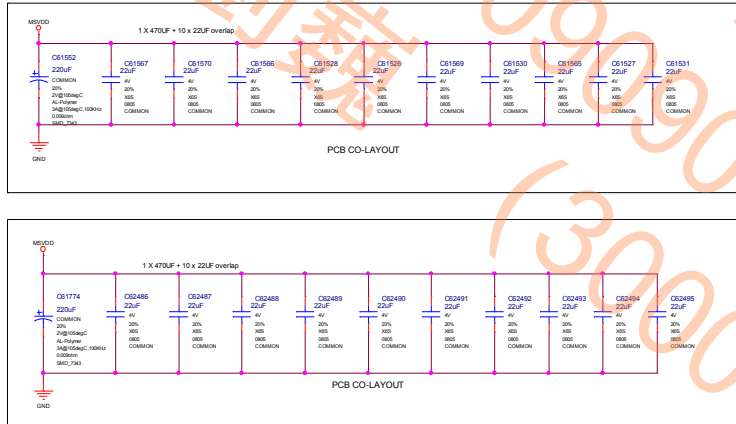
14x 0603 10uF



47x 0402 1uF




2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)

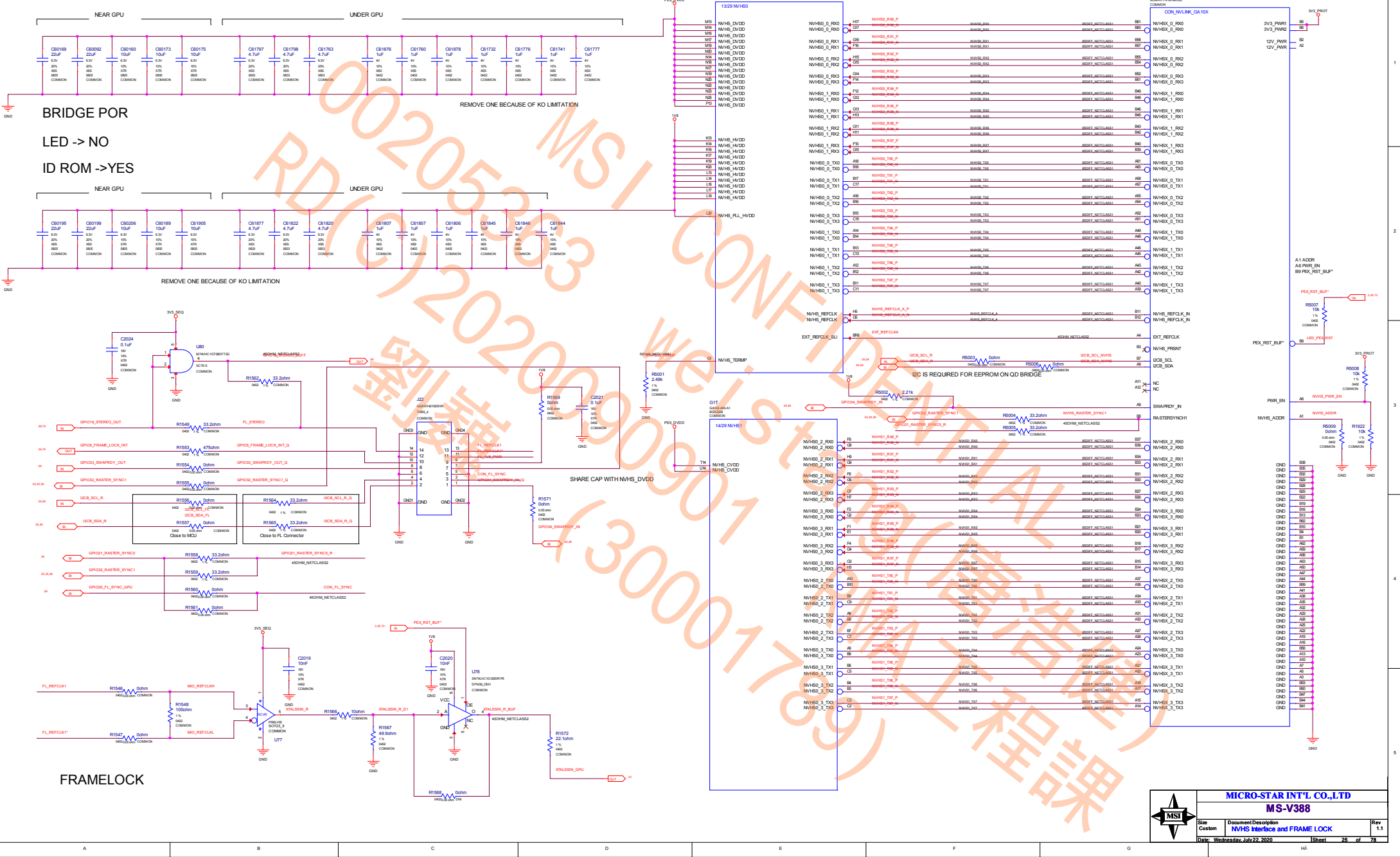


REMOVED 3x 1uF 0402 DUE TO SPACE RESTRICTION

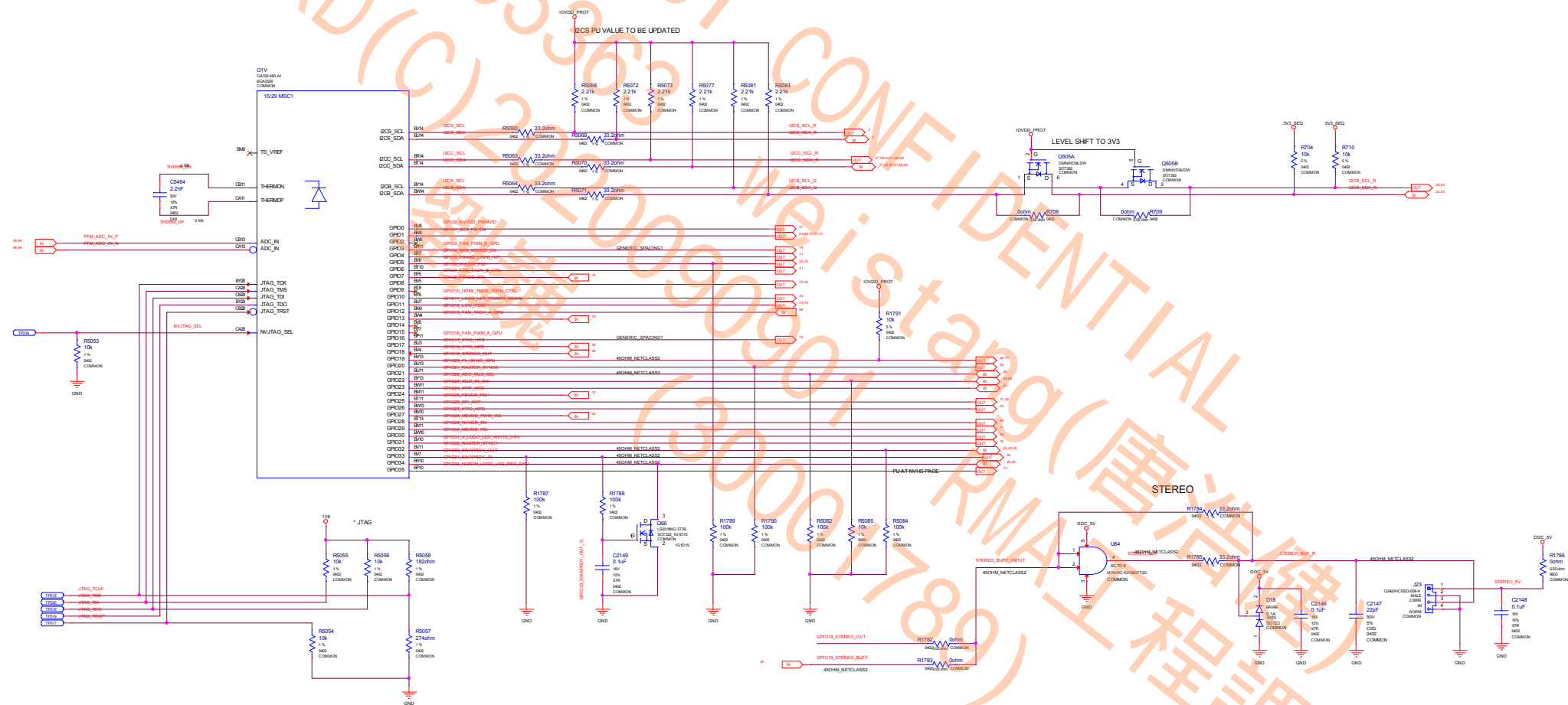
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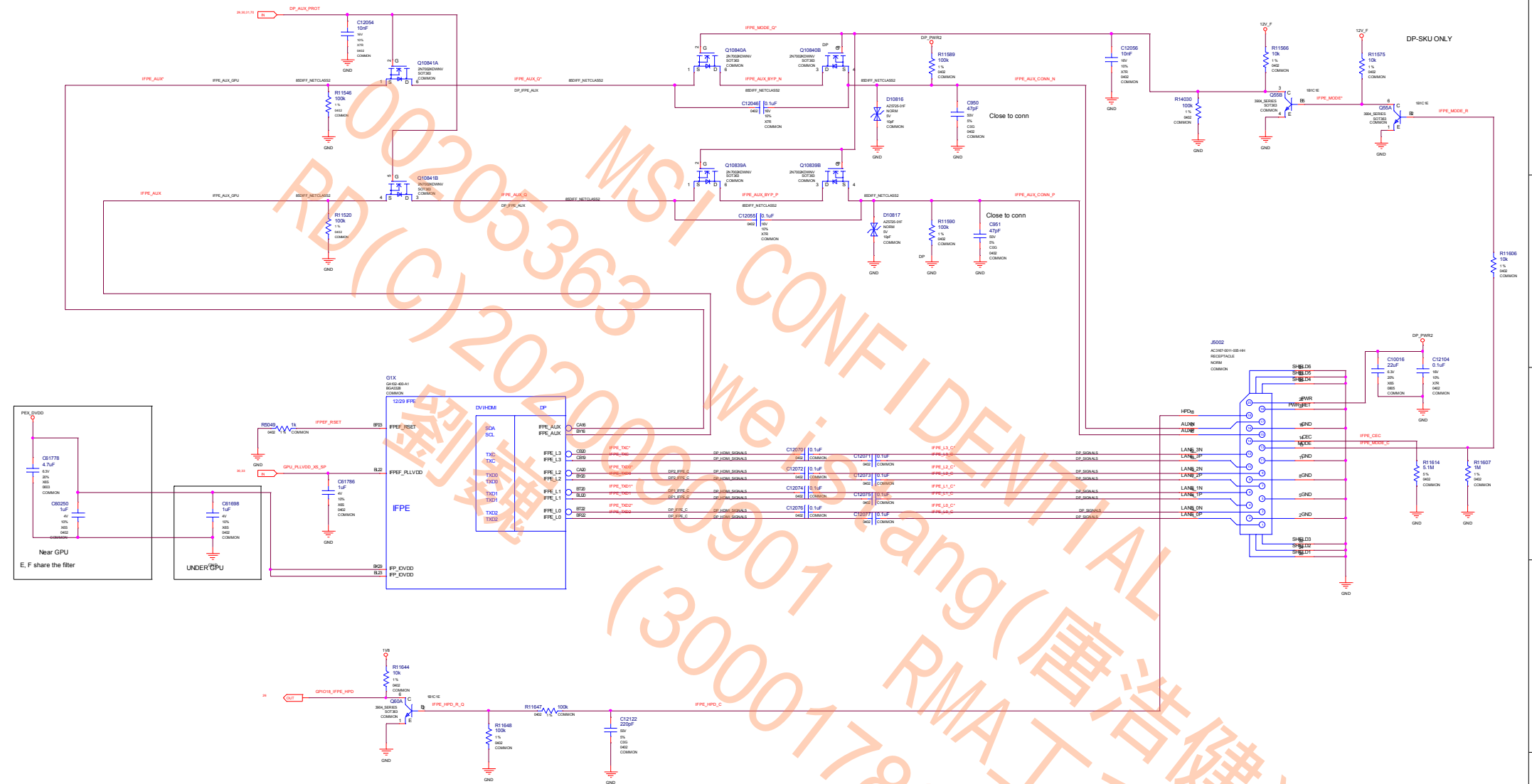
NVHS Interface and FRAME LOCK

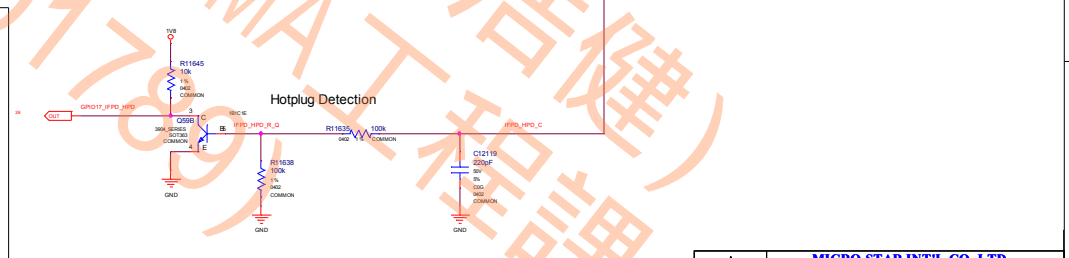
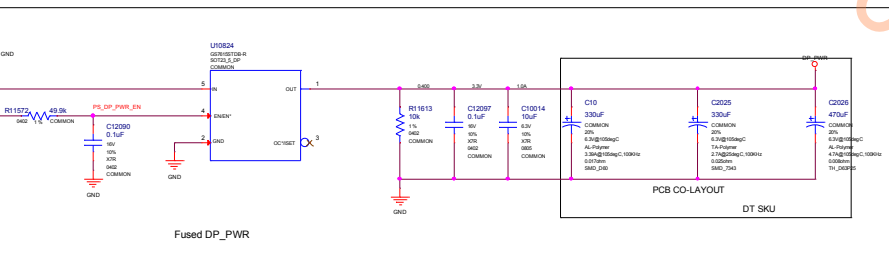
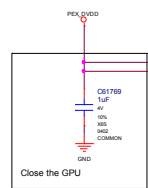
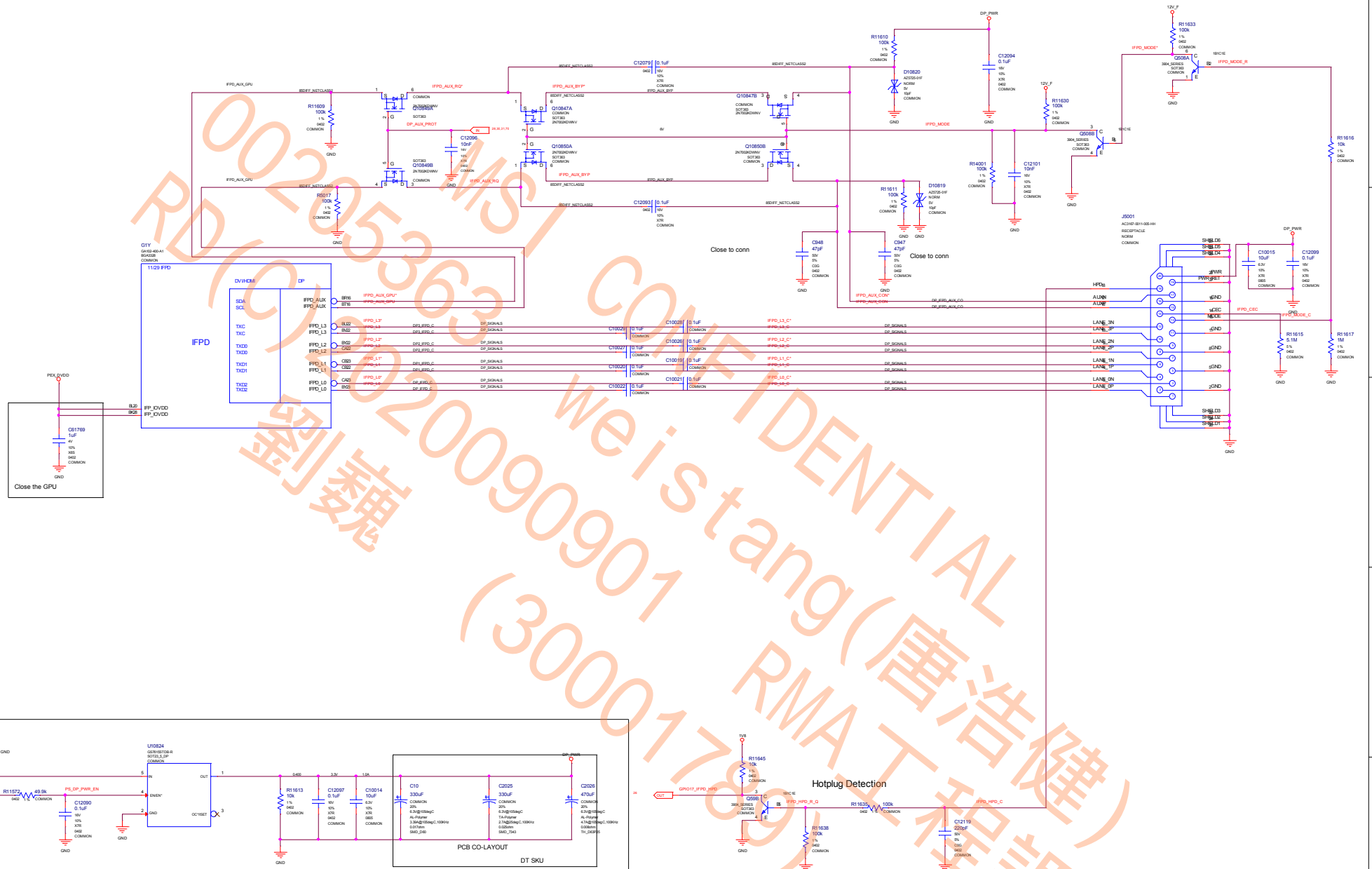


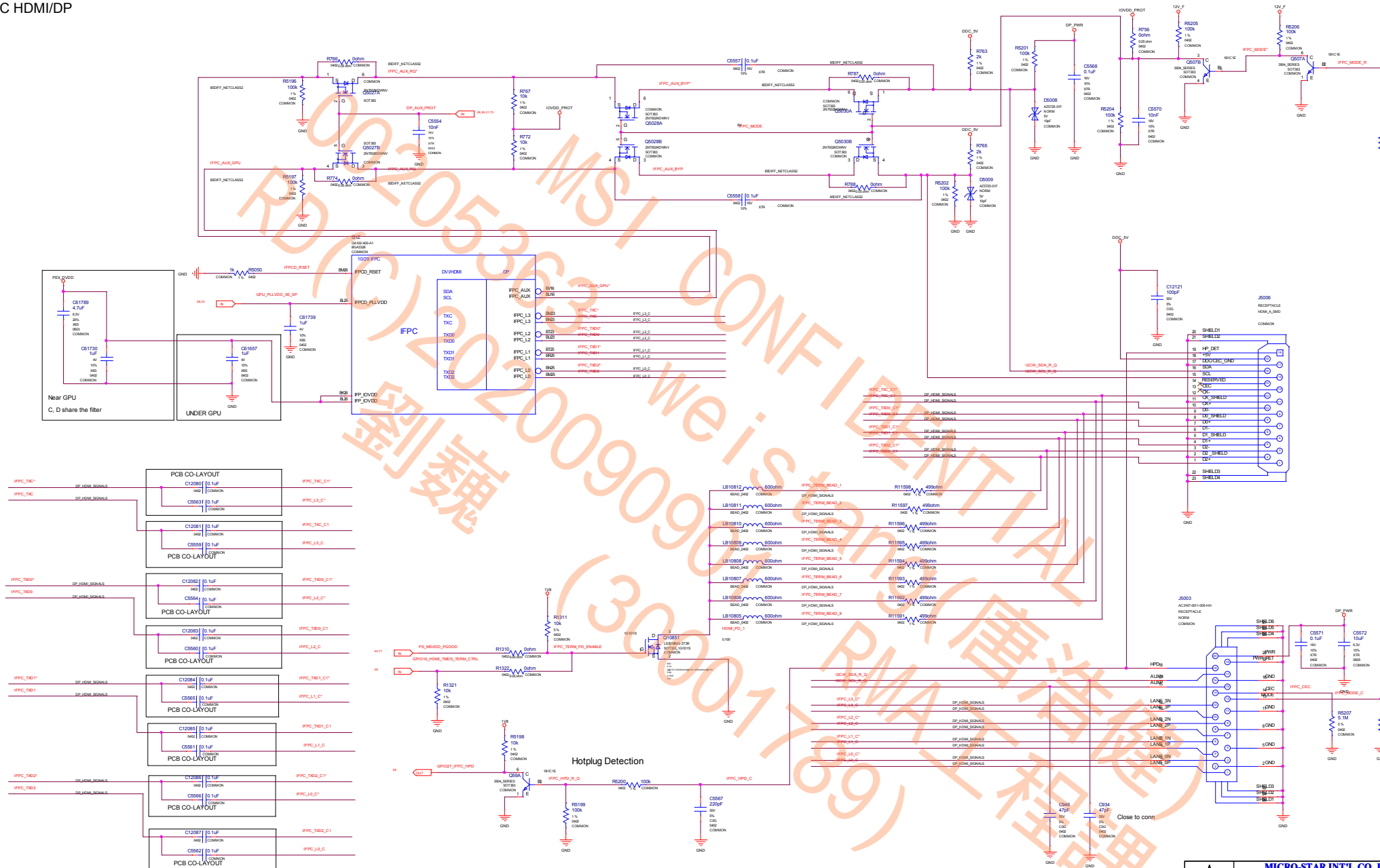
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



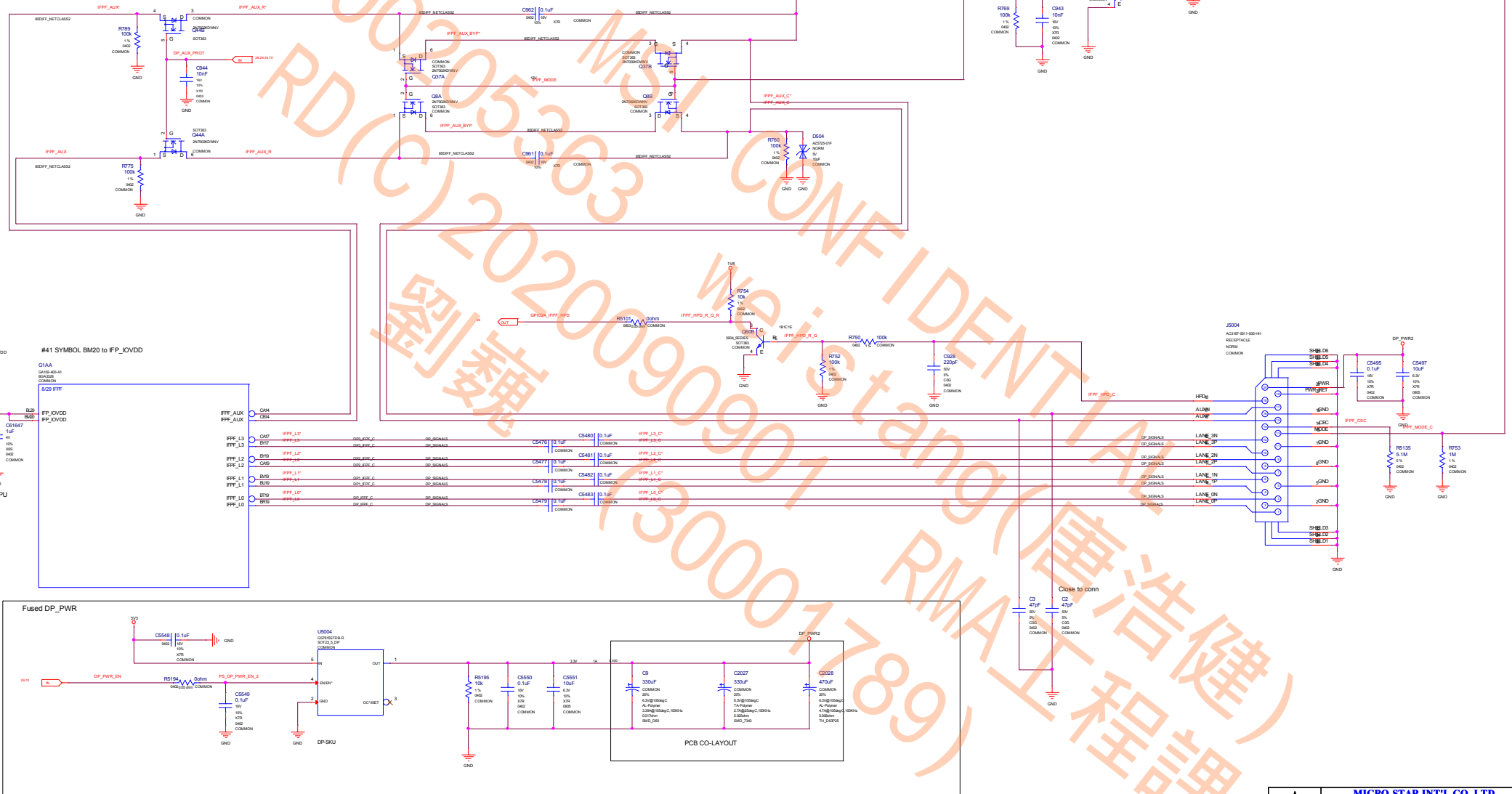
IFPE DP







IFPF DP



MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

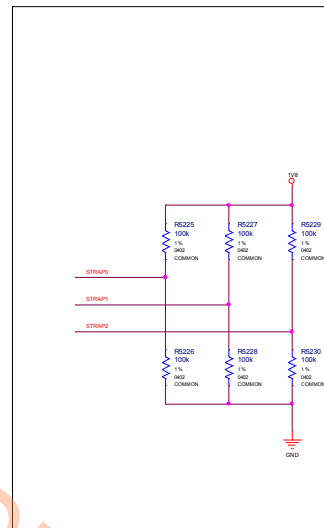
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

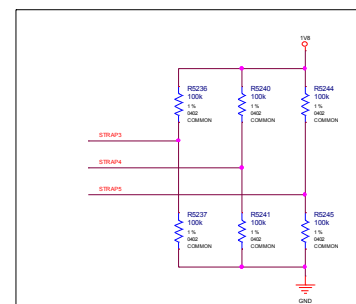
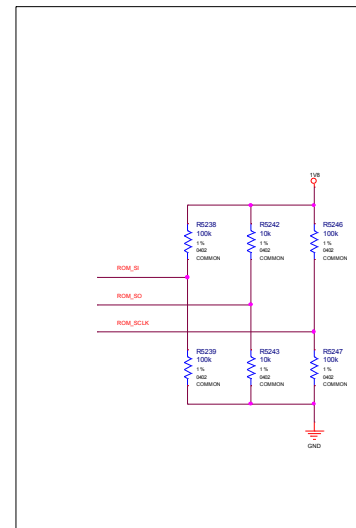
Default

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

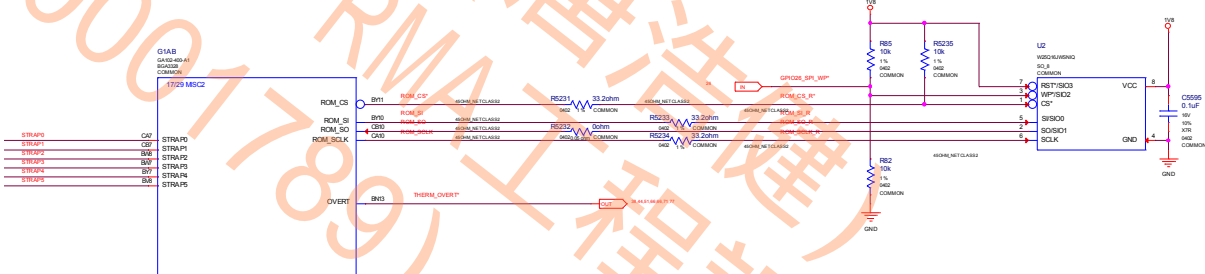
GROUP0

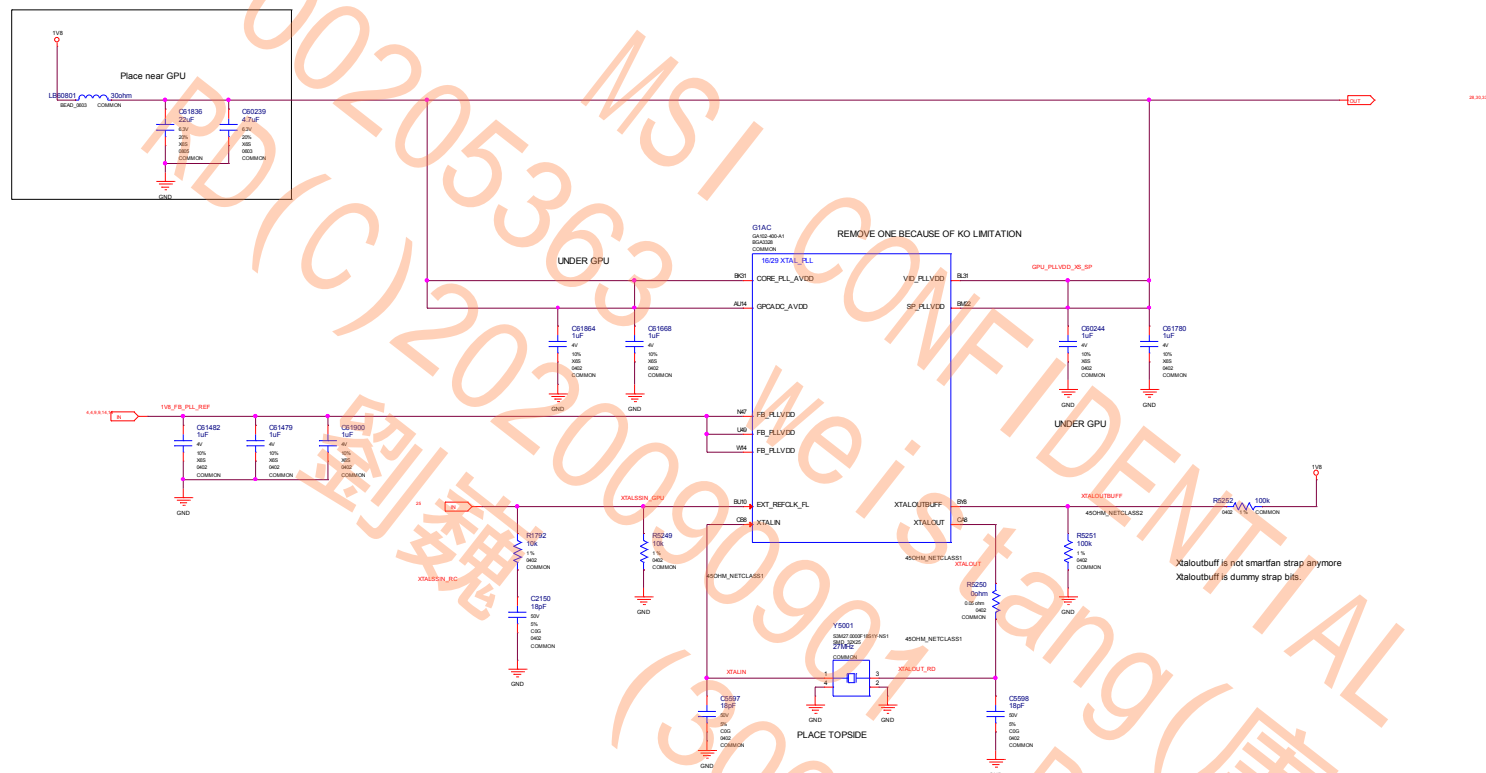


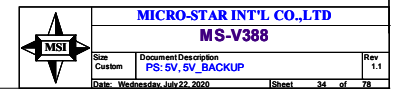
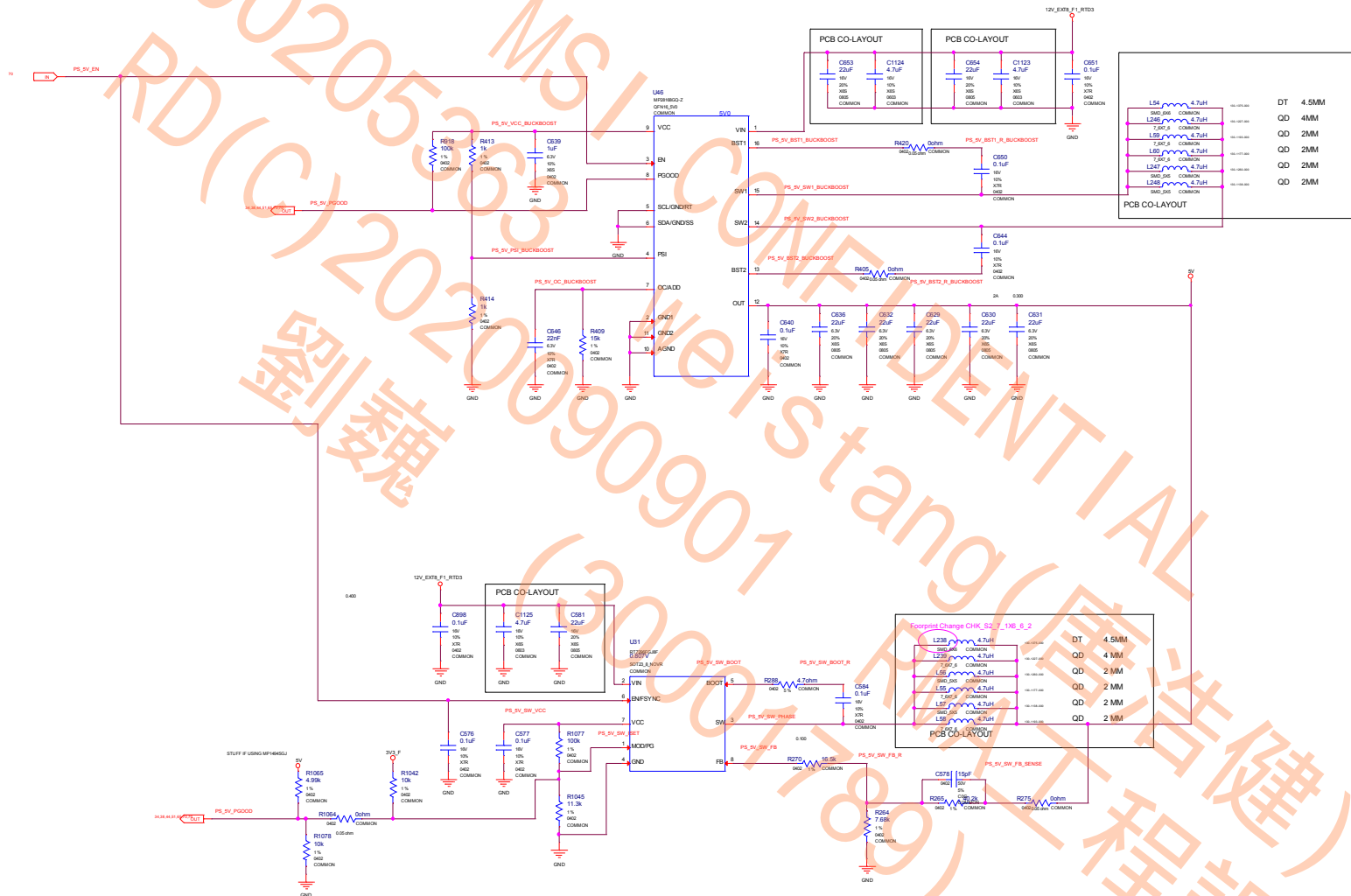
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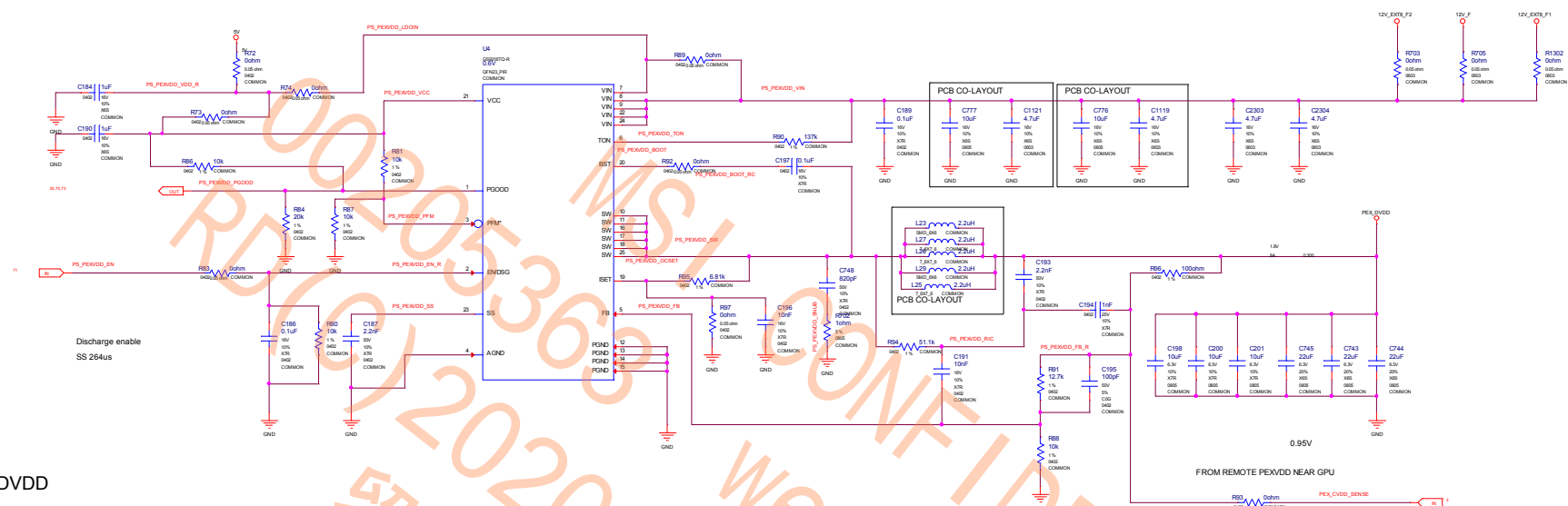


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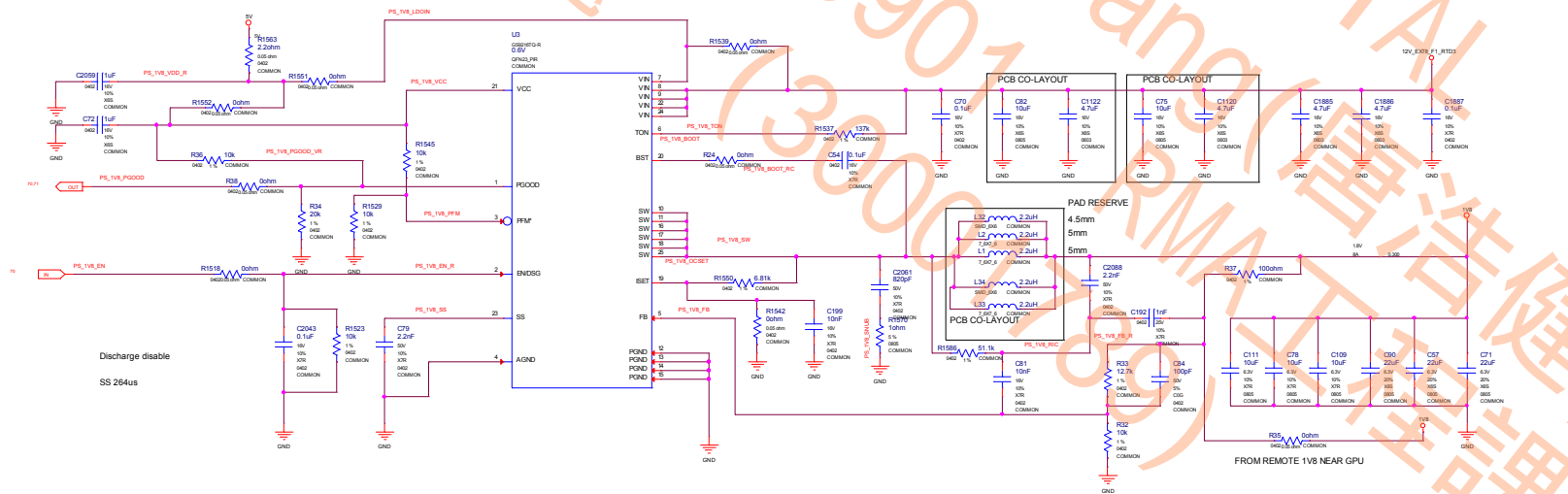








PEX_DVDD



1V8



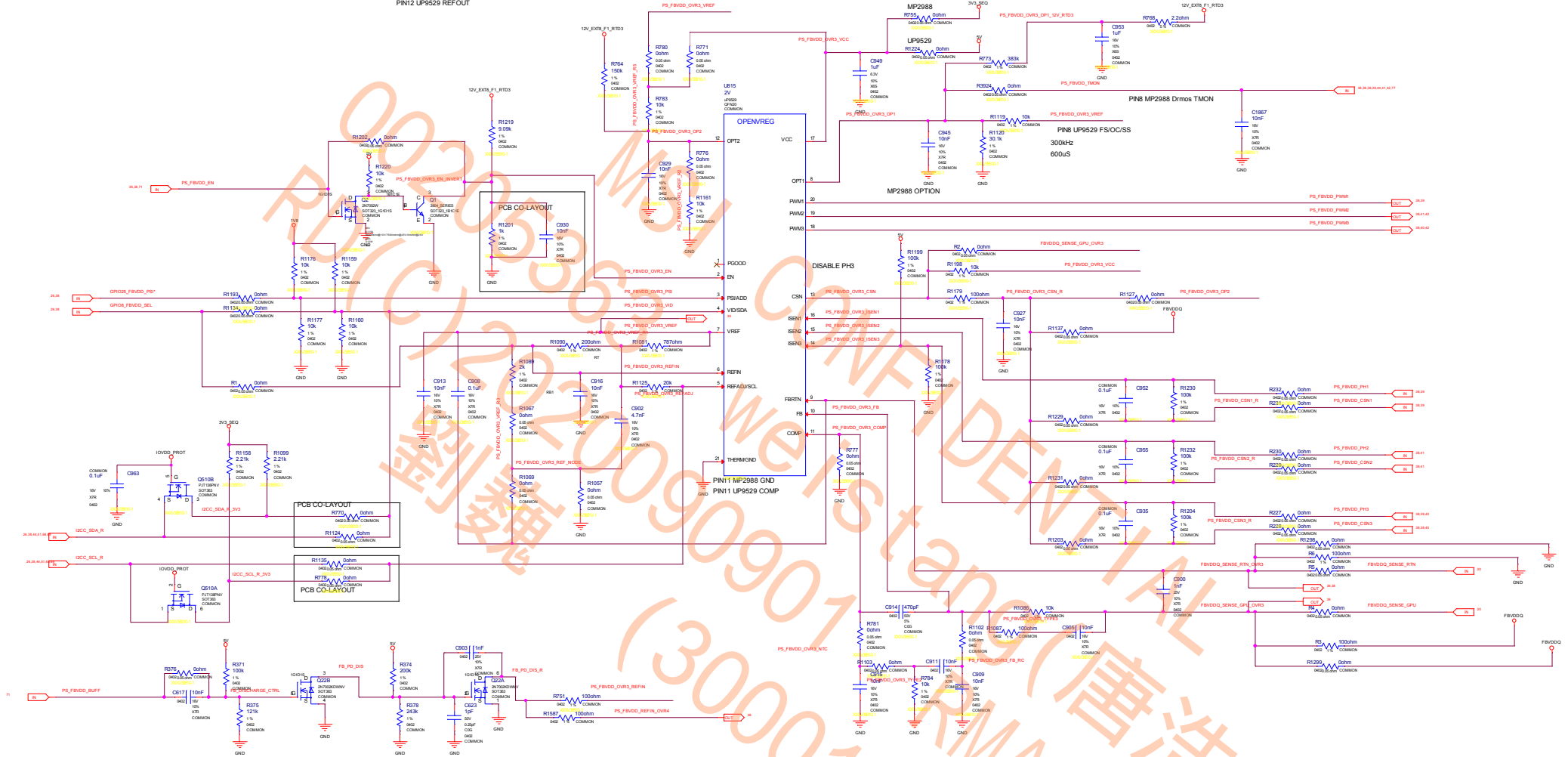
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RMA工程課

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PS: FBVDD Controller OVR3

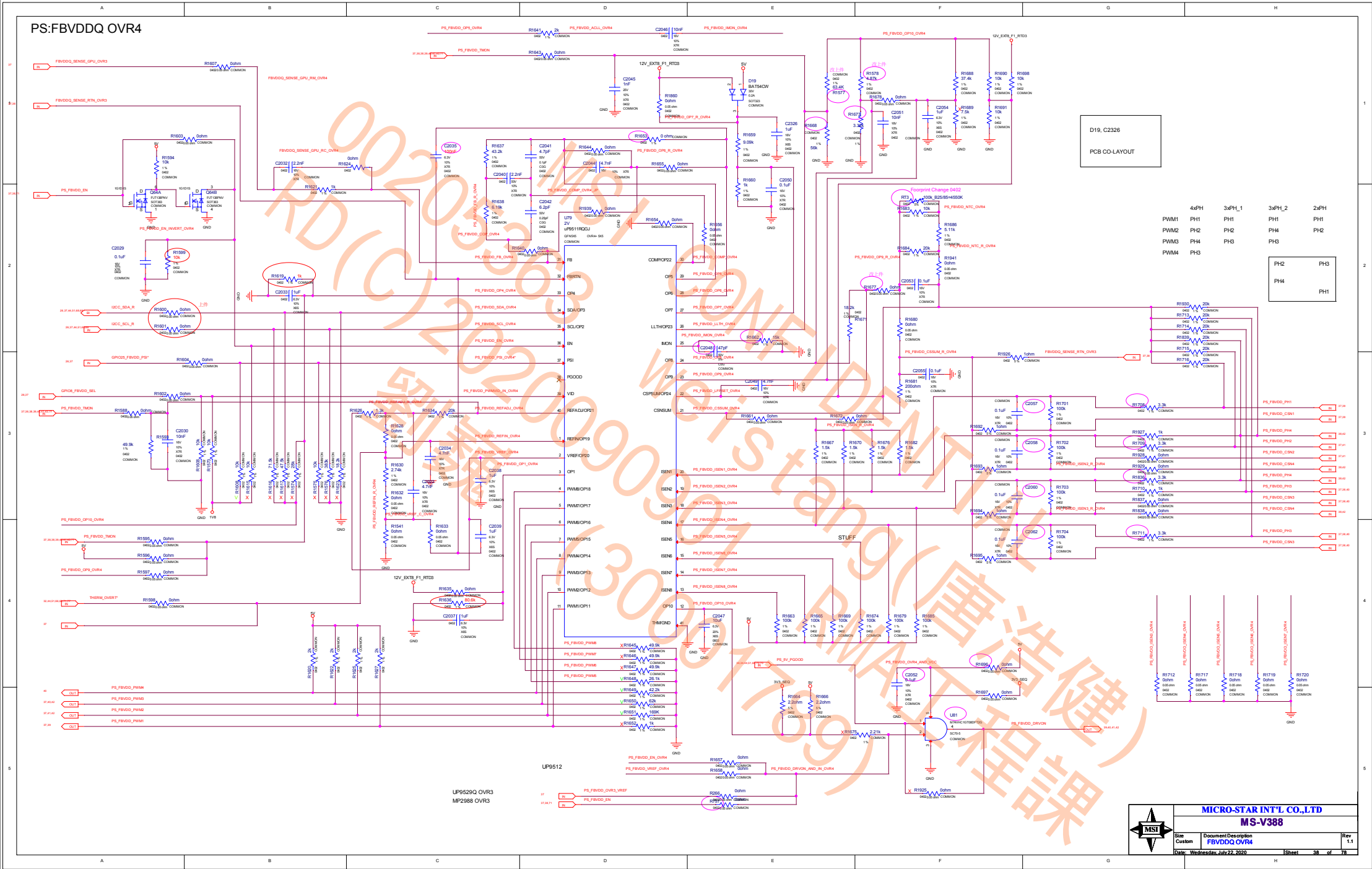
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PIN12 UP9529 REFOUT

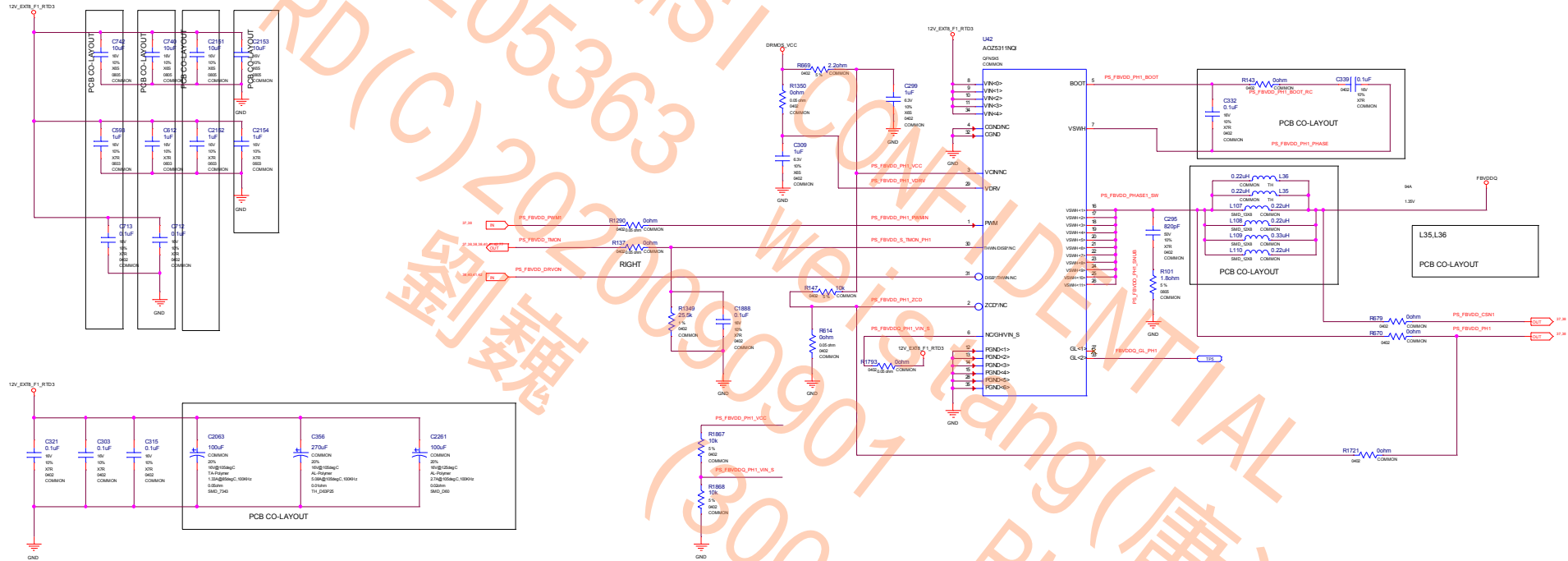


FOR DT SKU

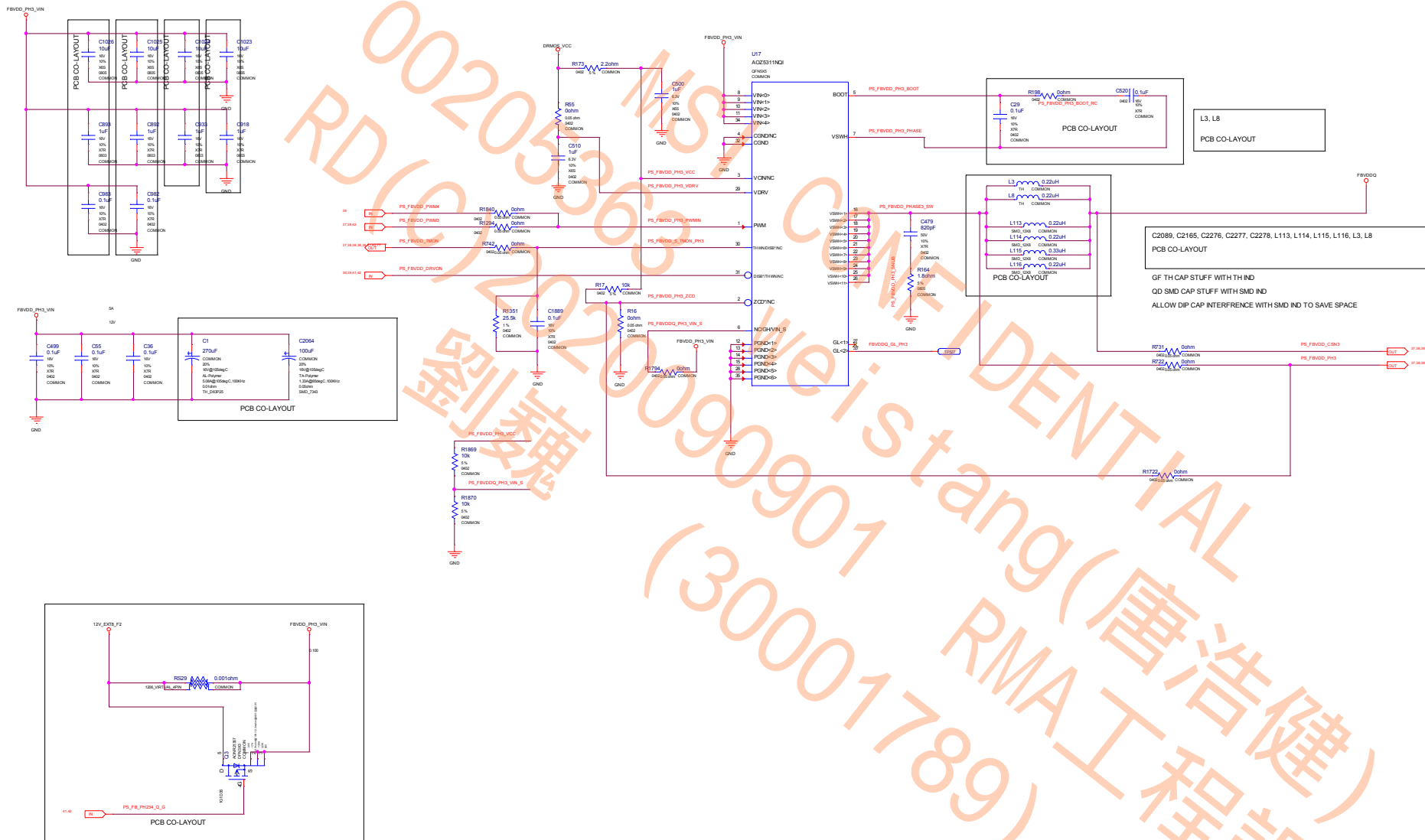
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PS:FBVDDQ OVR4





PS: FBVDD PH3

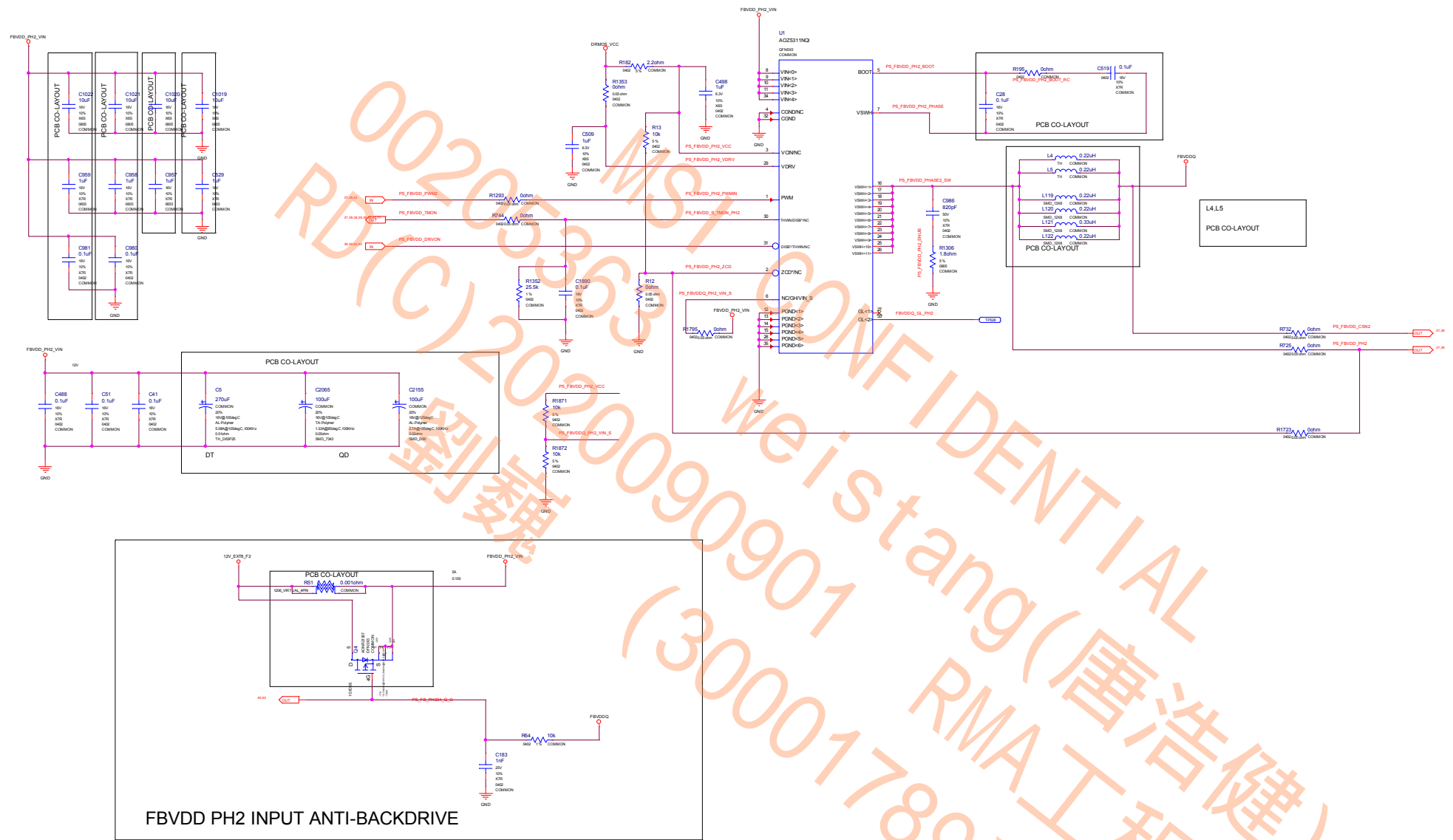


FBVDD PH3 INPUT ANTI-BACKDRIVE

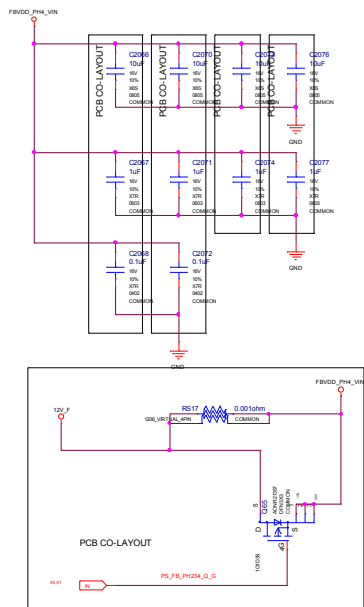


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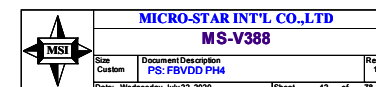
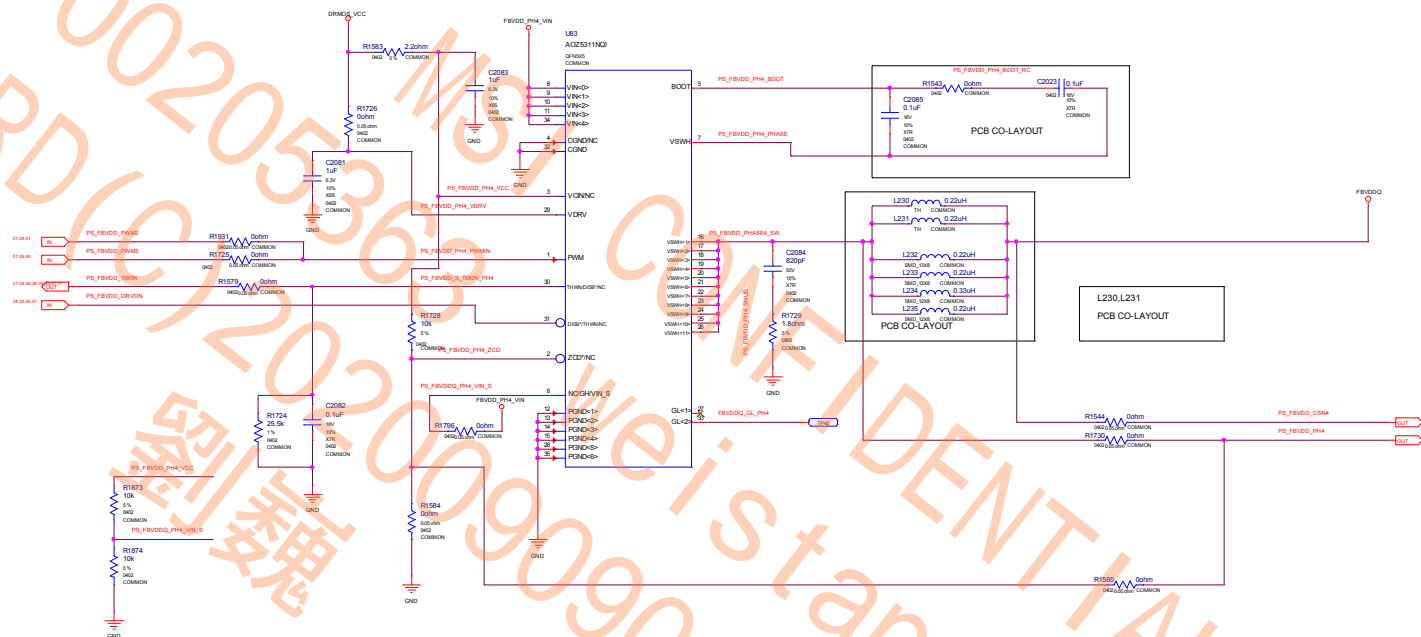
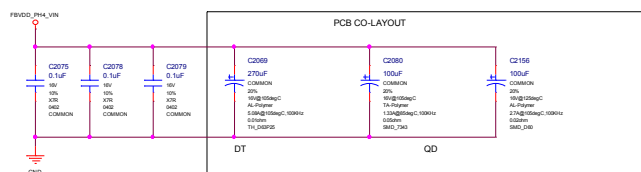
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PS: FBVDD PH4

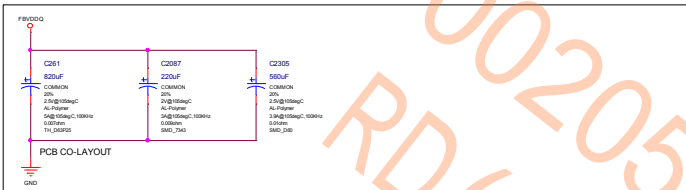


FBVDD PH3 INPUT ANTI-BACKDRIVE



REFER TO PCB FOR BOM STUFFING

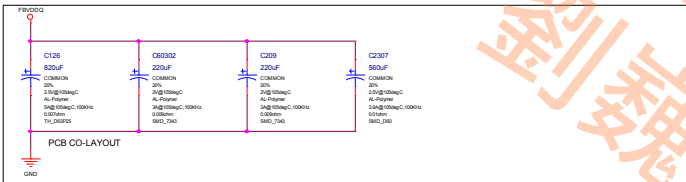
PH1 TOP



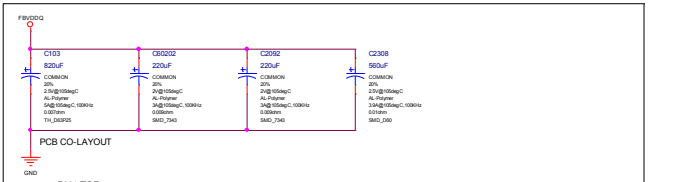
PH3 TOP



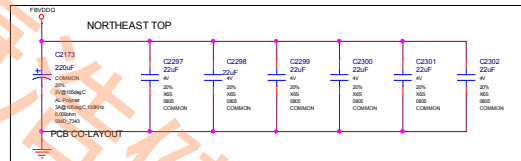
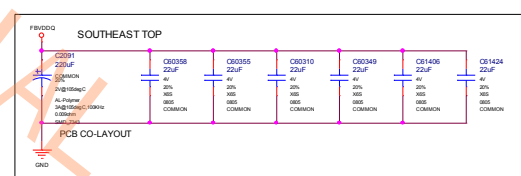
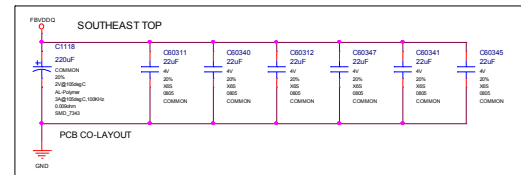
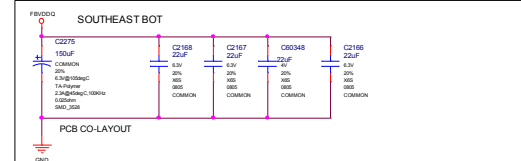
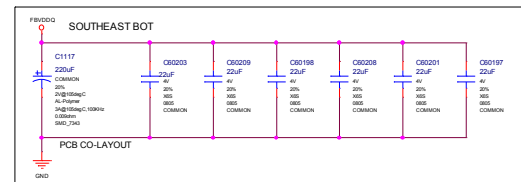
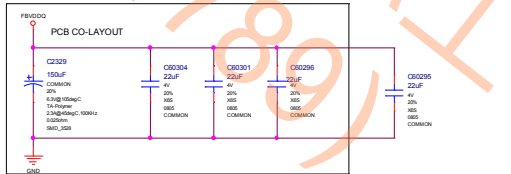
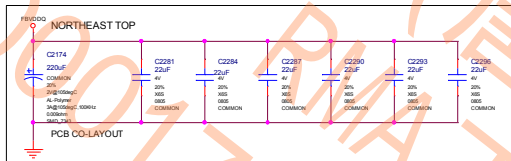
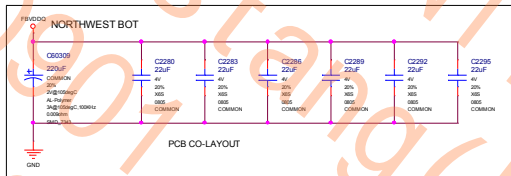
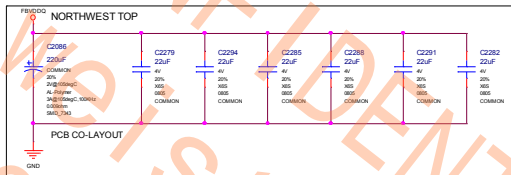
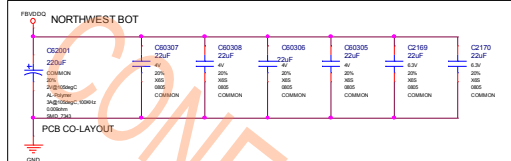
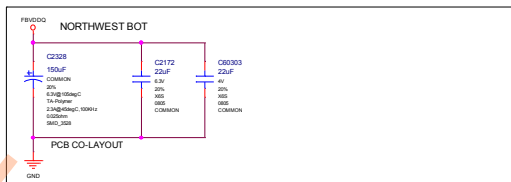
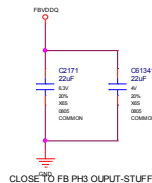
PH2 TOP



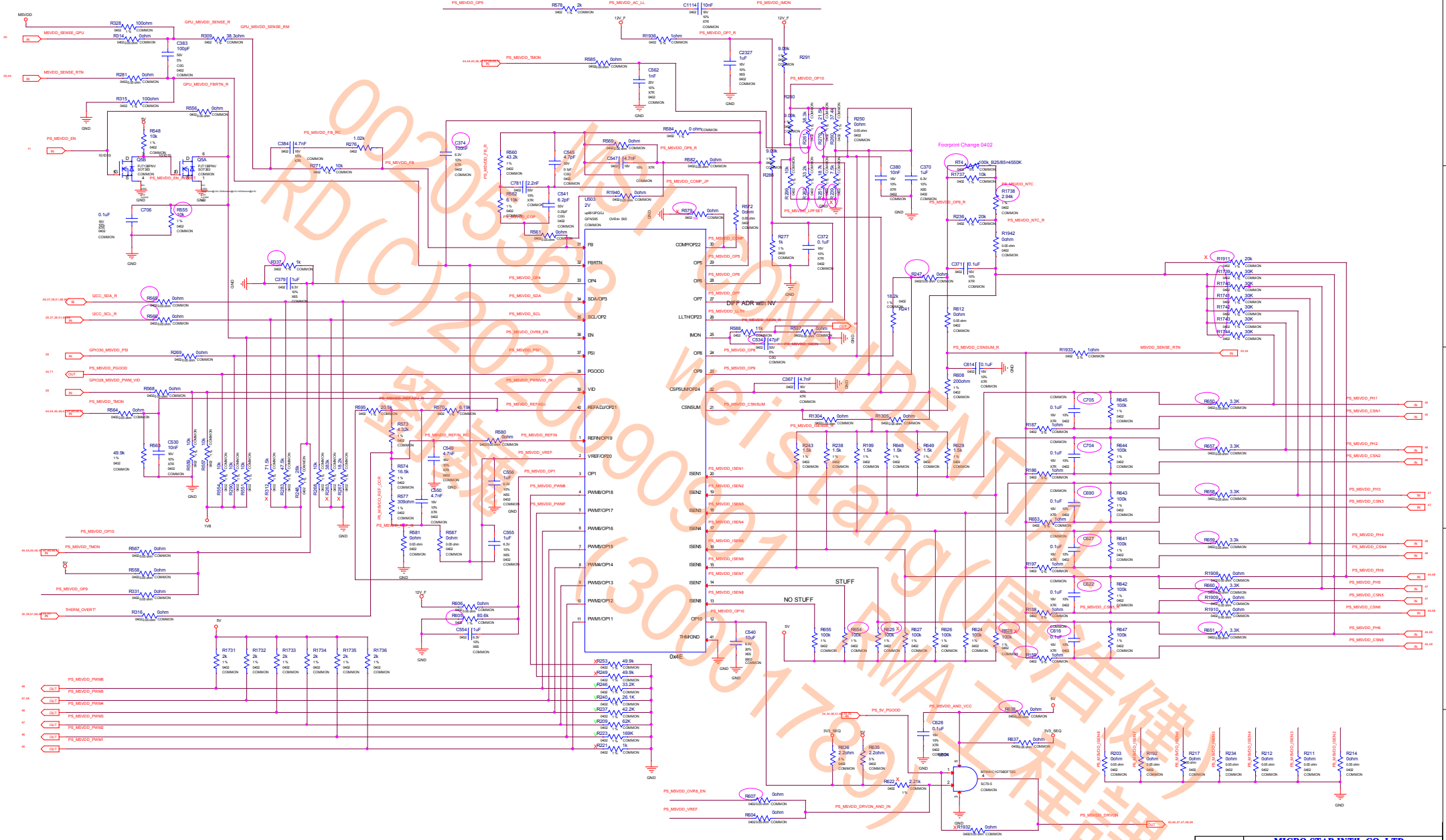
PH4 TOP



PH4 TOP



PS: MSVDD



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MS-V388

Size	Cost
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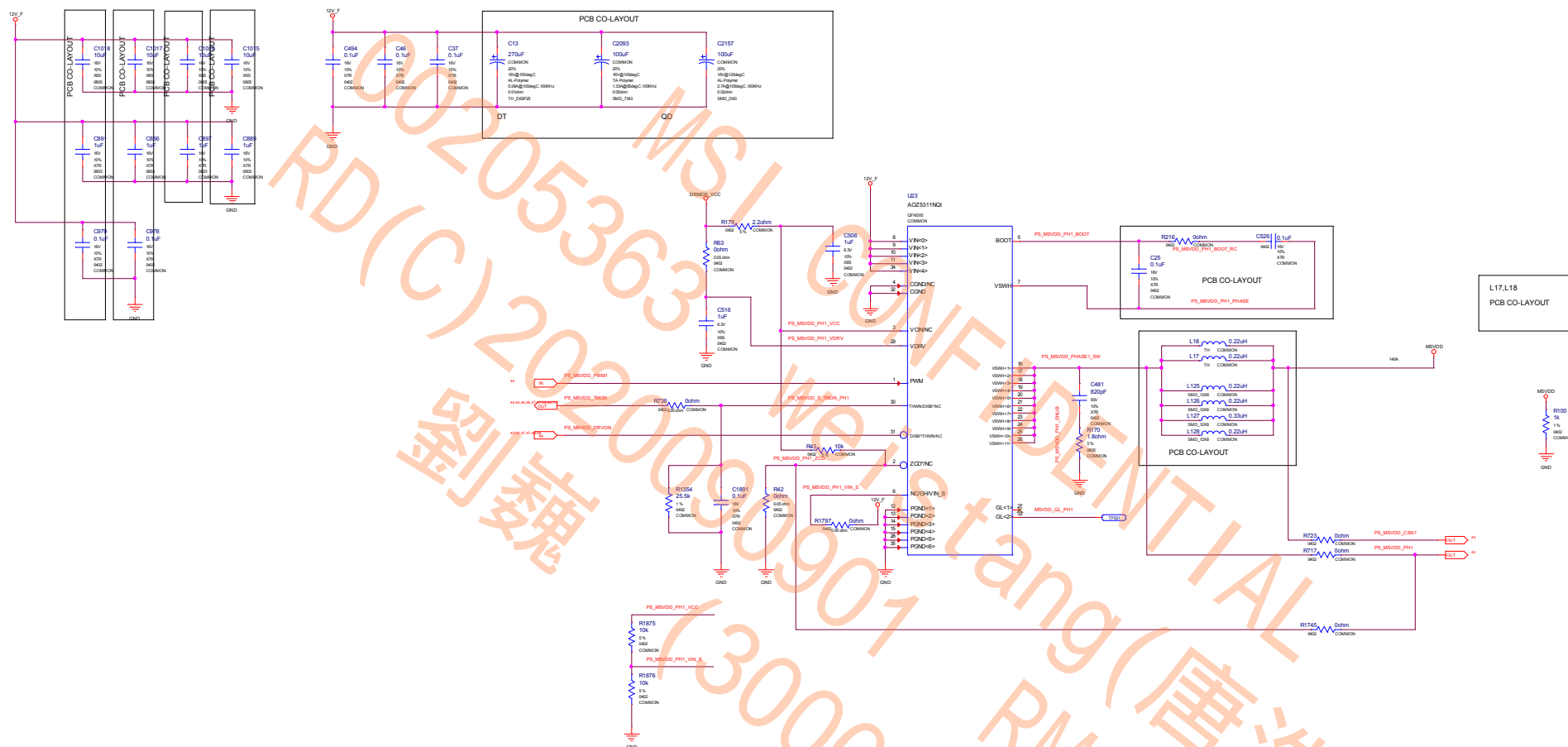
Document Description
RS: MSVDD

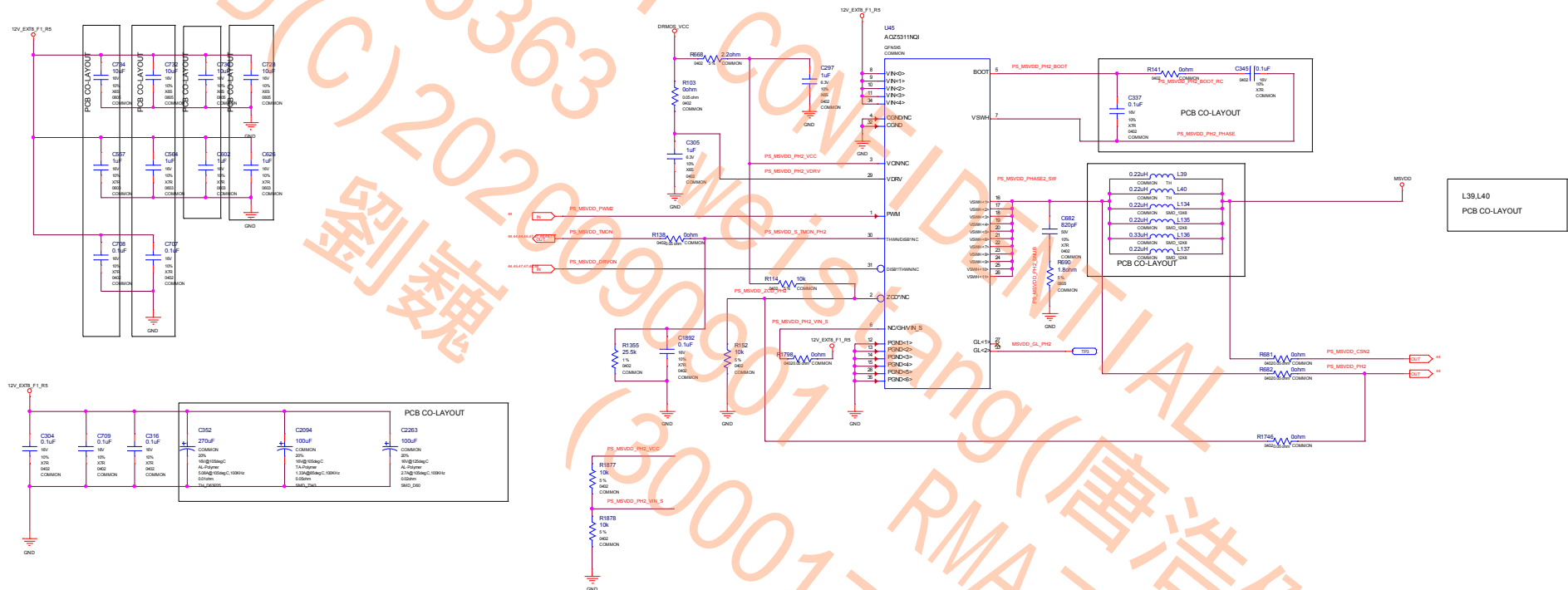
Cust#	
Date	

Wednesday, July 26, 2006

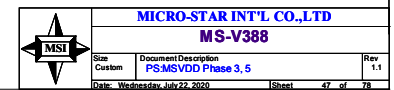
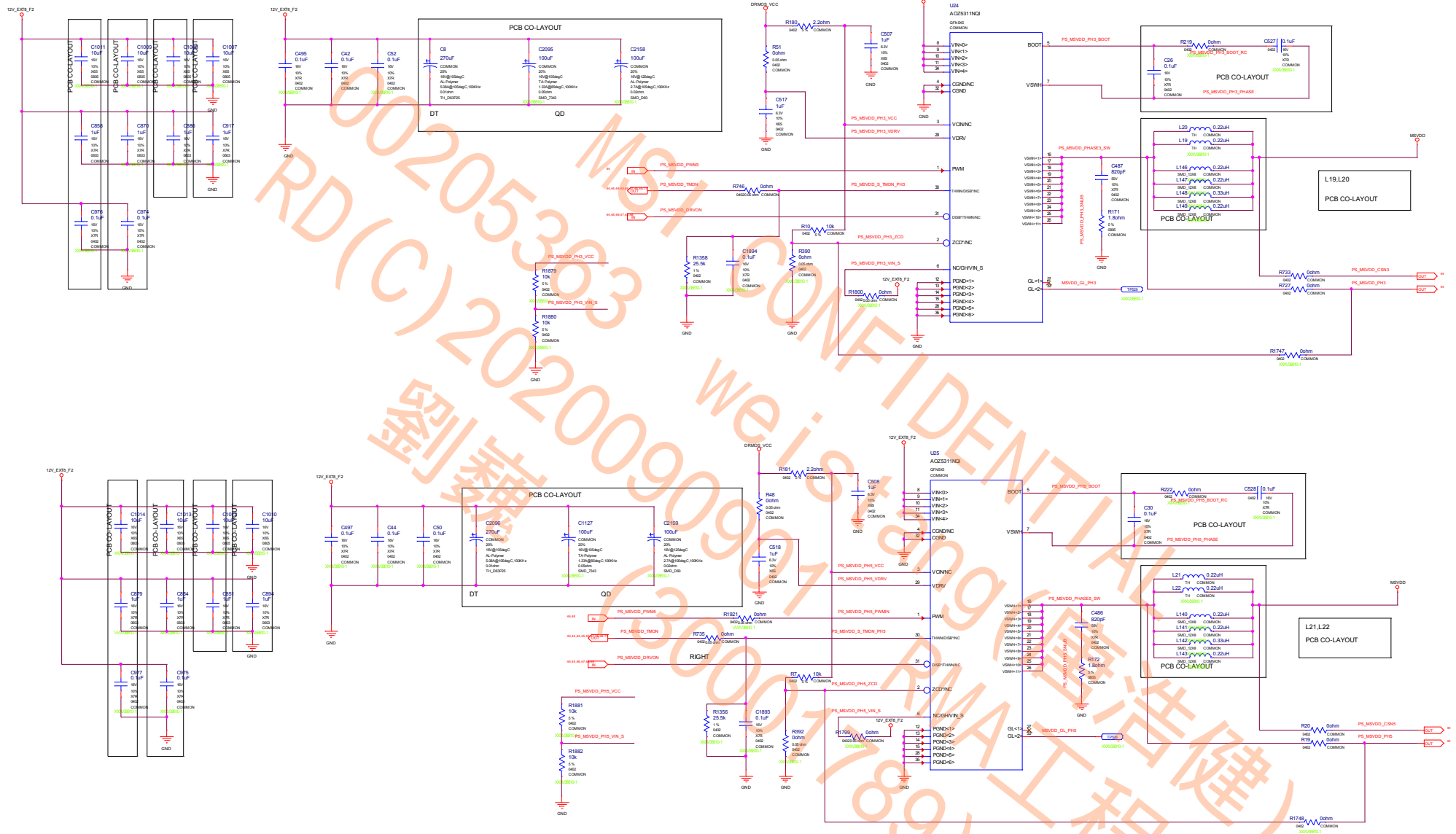
Rev	1.1
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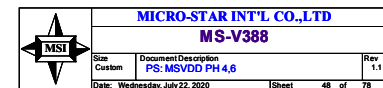
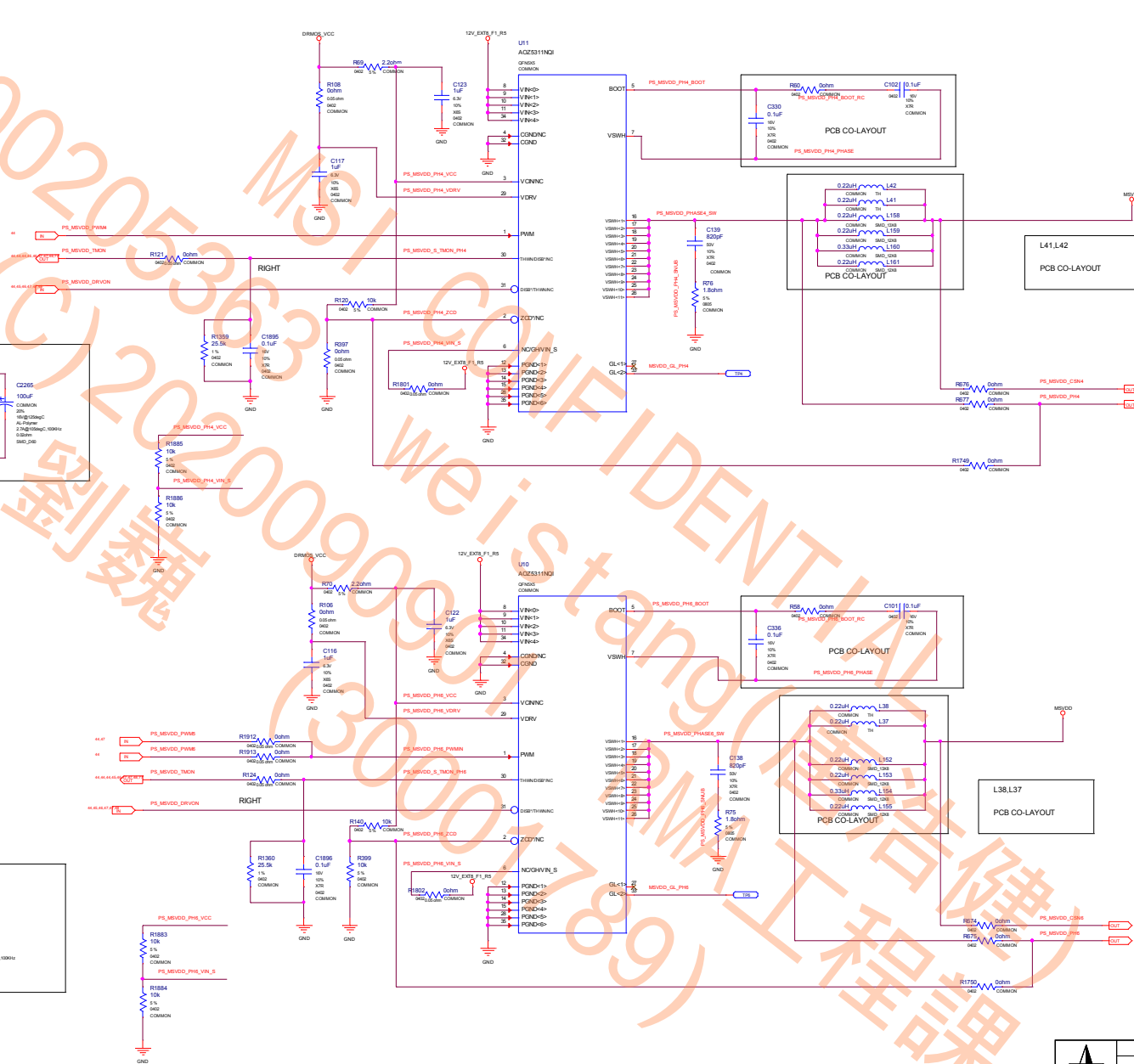
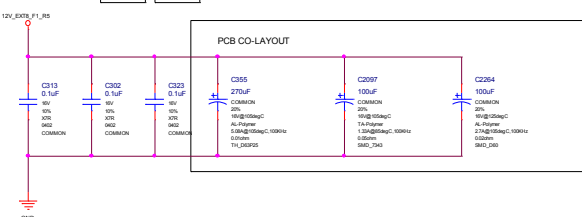
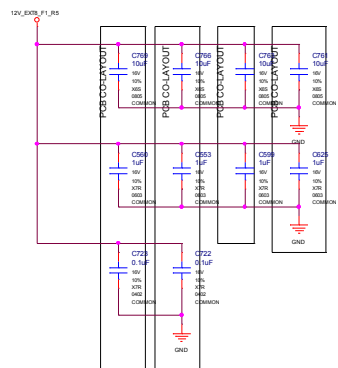
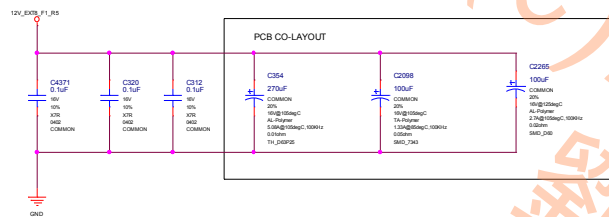
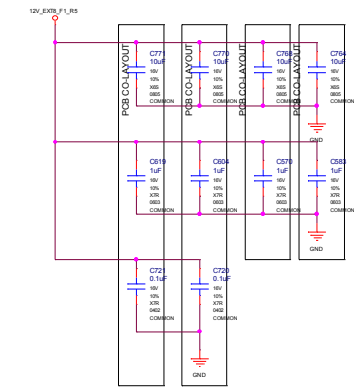
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10	



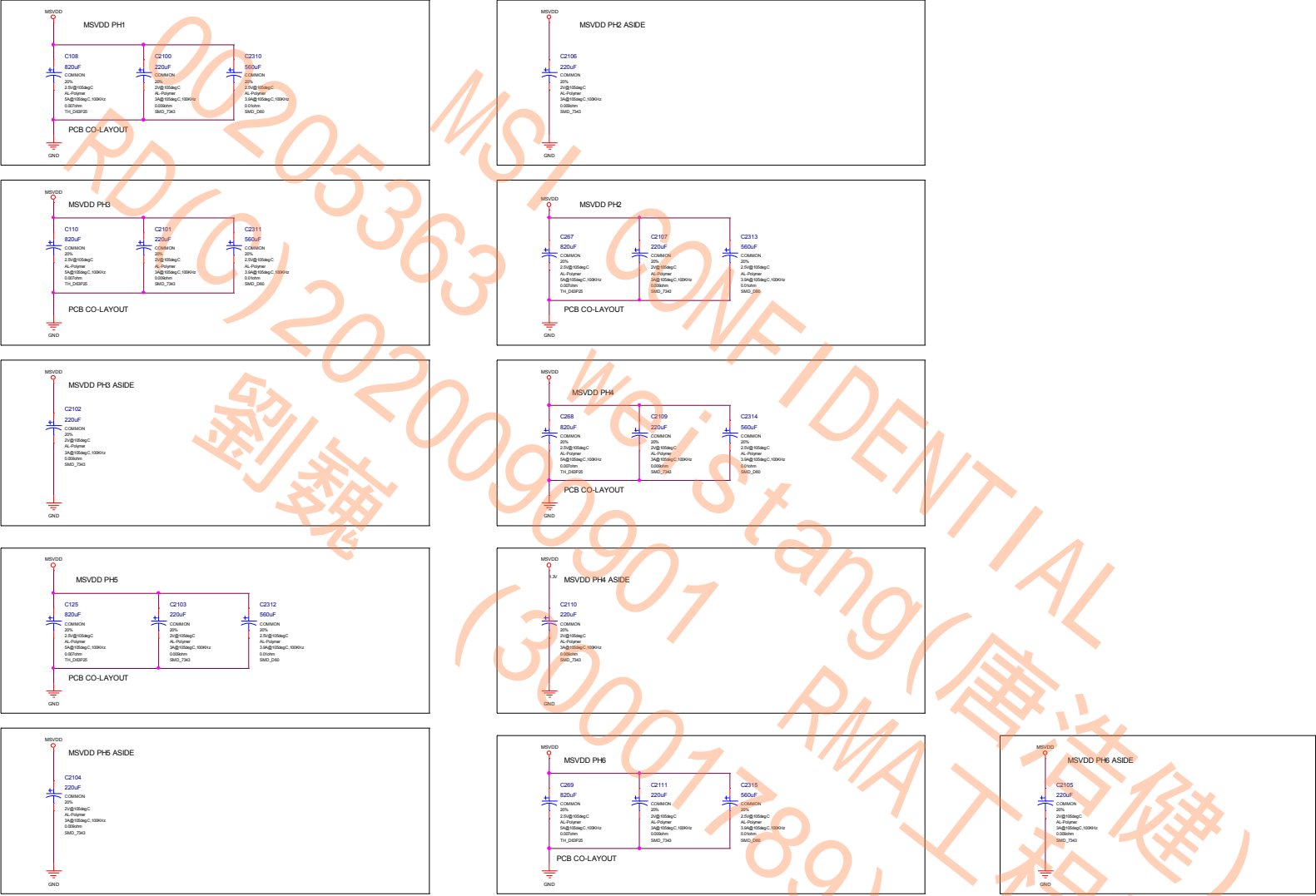


PS:MSVDD Phase 3, 5






REFER TO PCB FOR BOM STUFFING

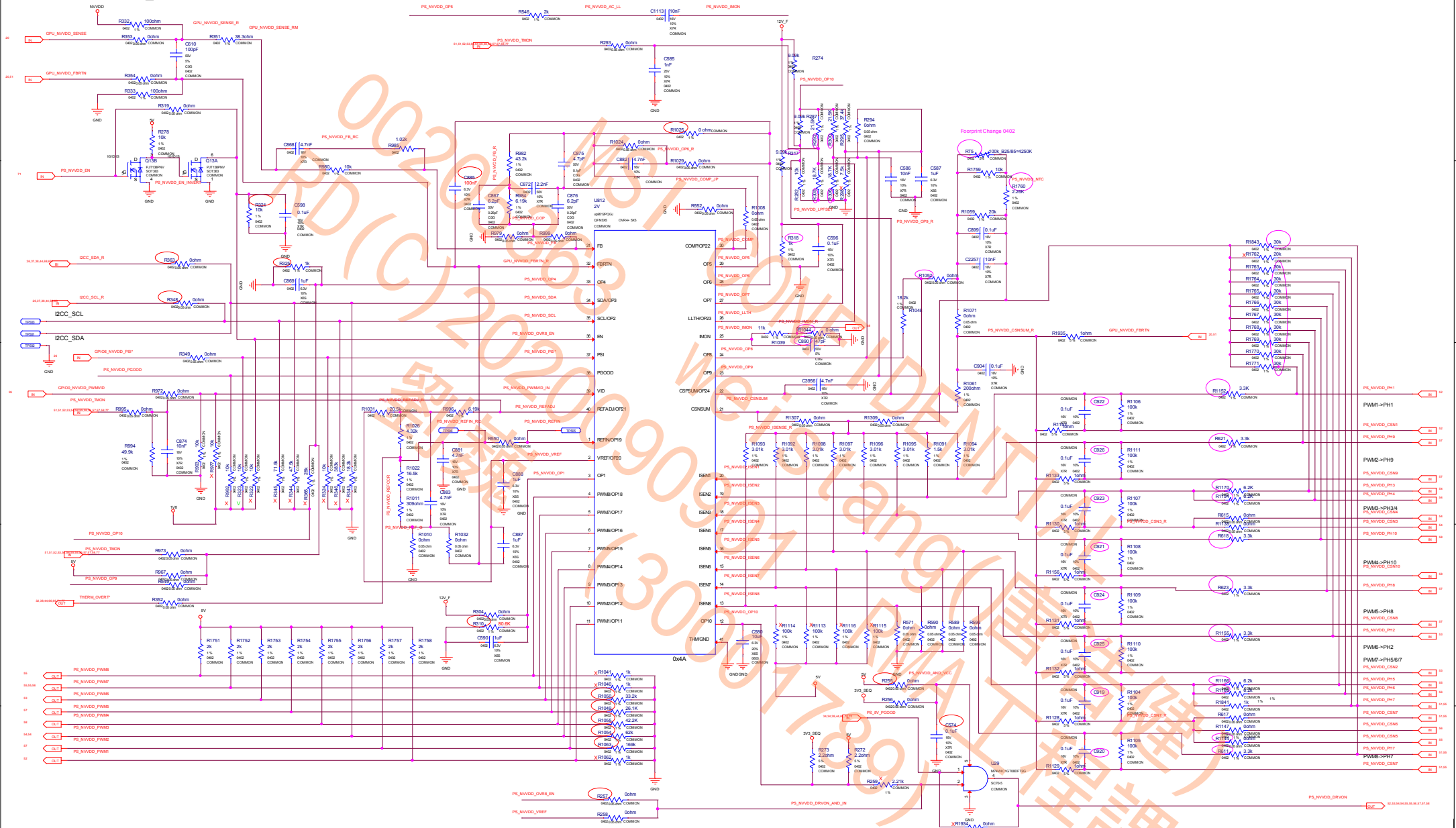


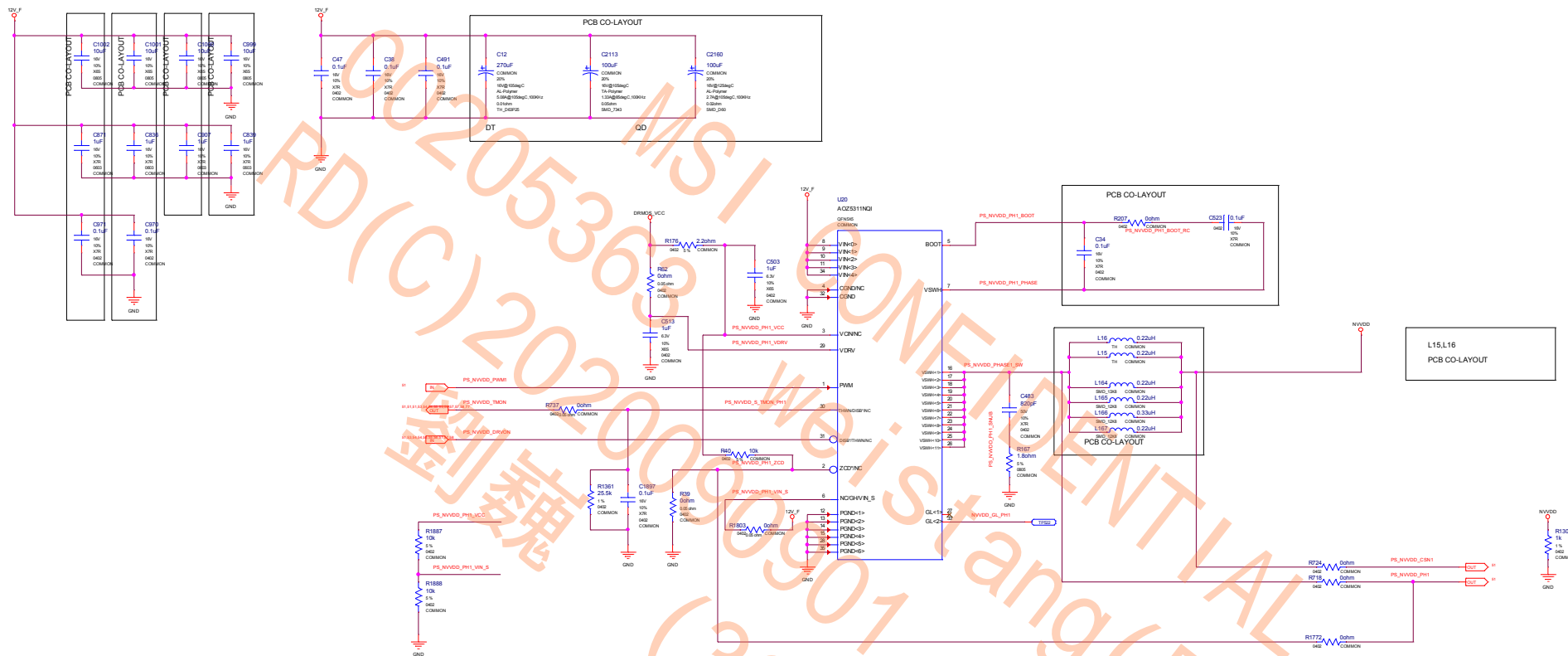
MSI CONFIDENTIAL
00205363
RD(C)2020090901
Weistang (唐浩健)
(30001789)
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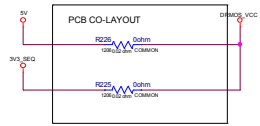
			MICRO-STAR INT'L CO.,LTD	
			MS-V388	
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PS: NVVDD Controller_OVR8

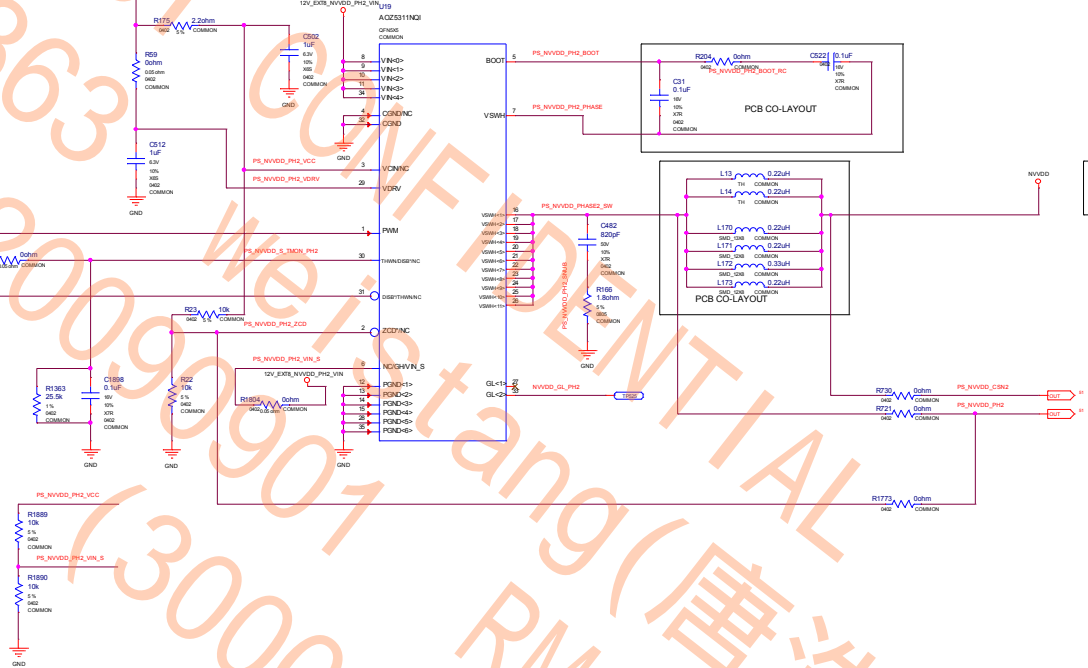
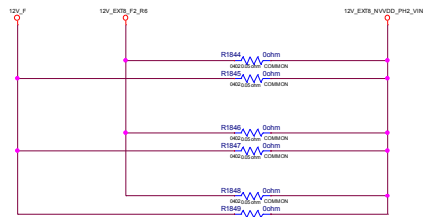
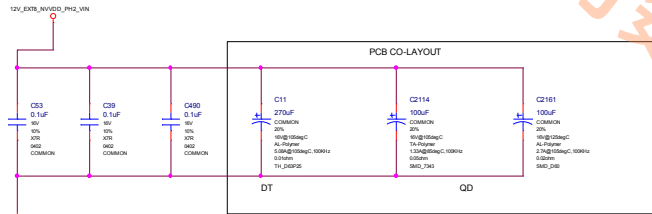
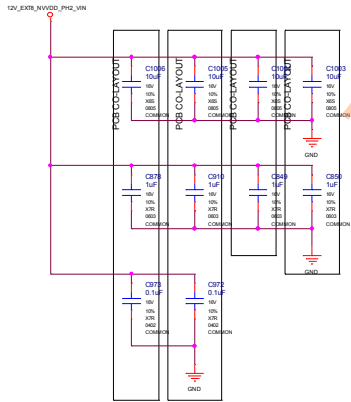




PS: NVVDD Phase 2 (PWM6)

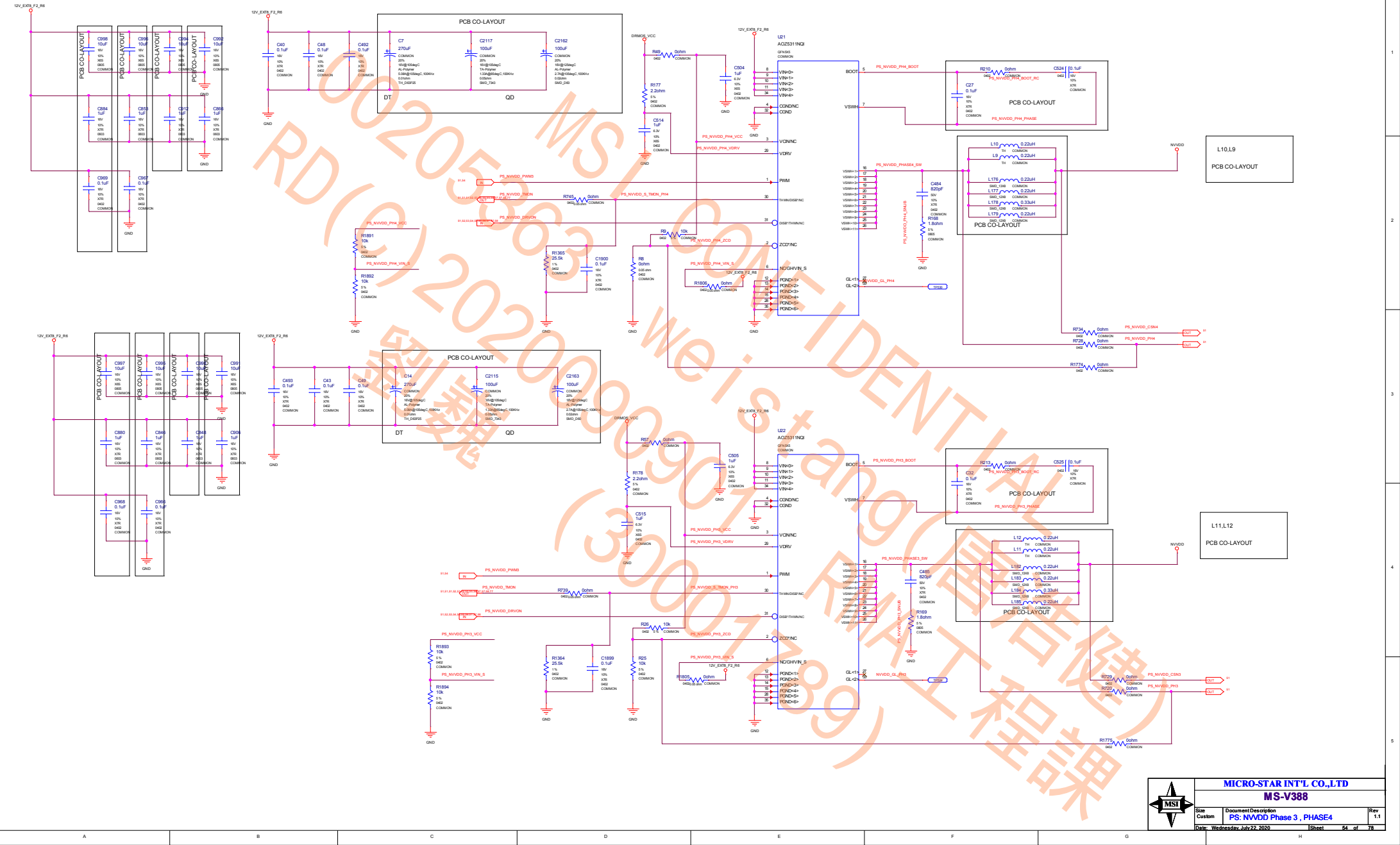


MPS DRMOS WITH 3V3 SUPPLY

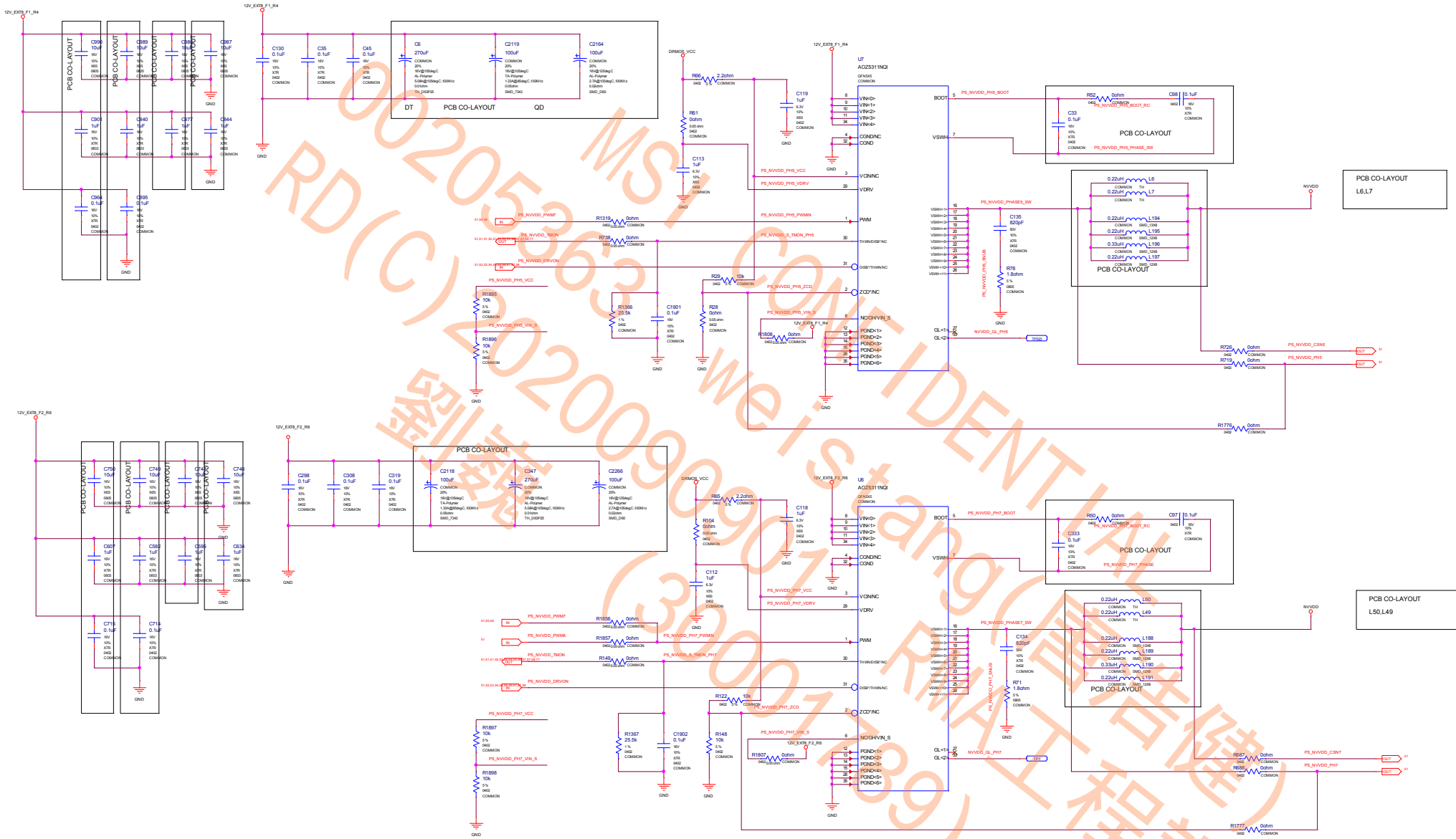


L13,L14
PCB CO-LAYOUT

PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



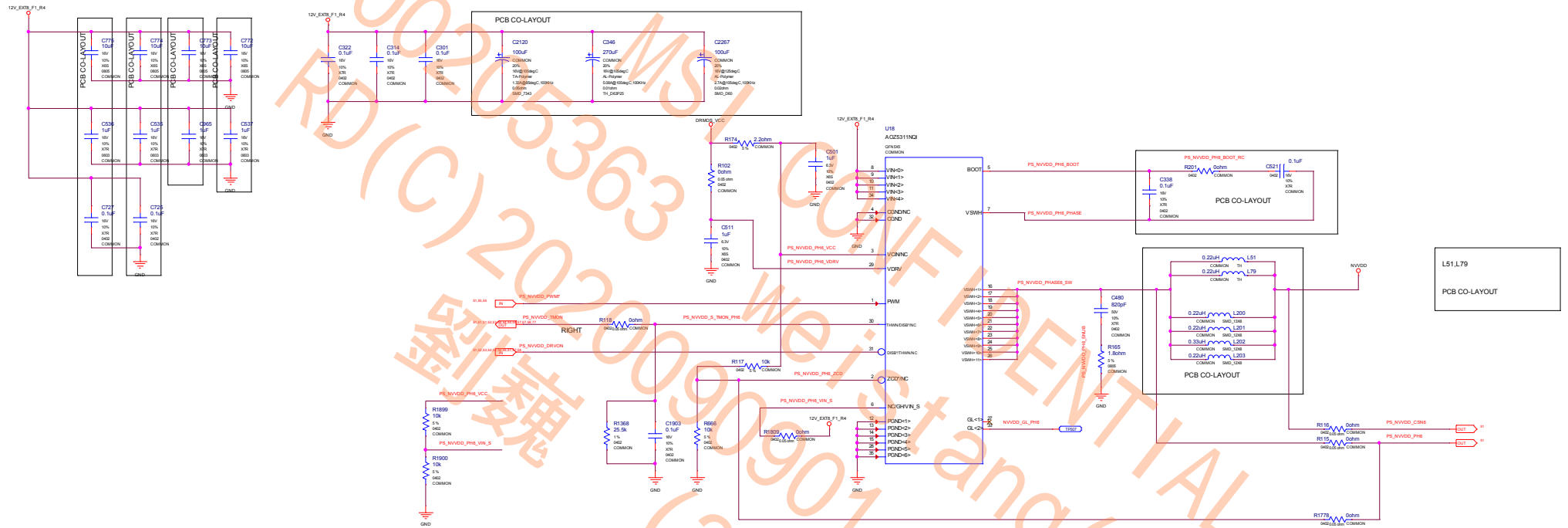
PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



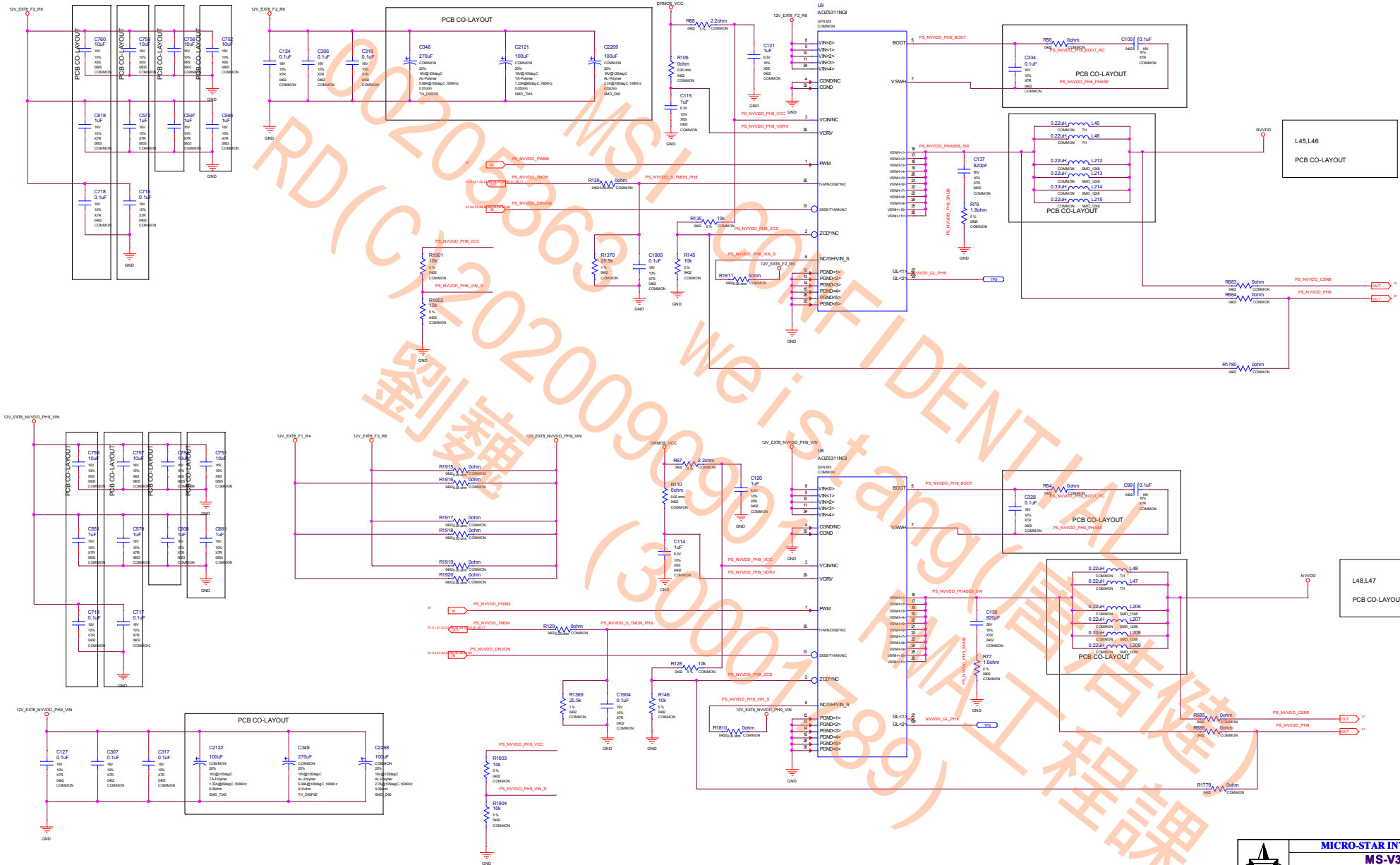
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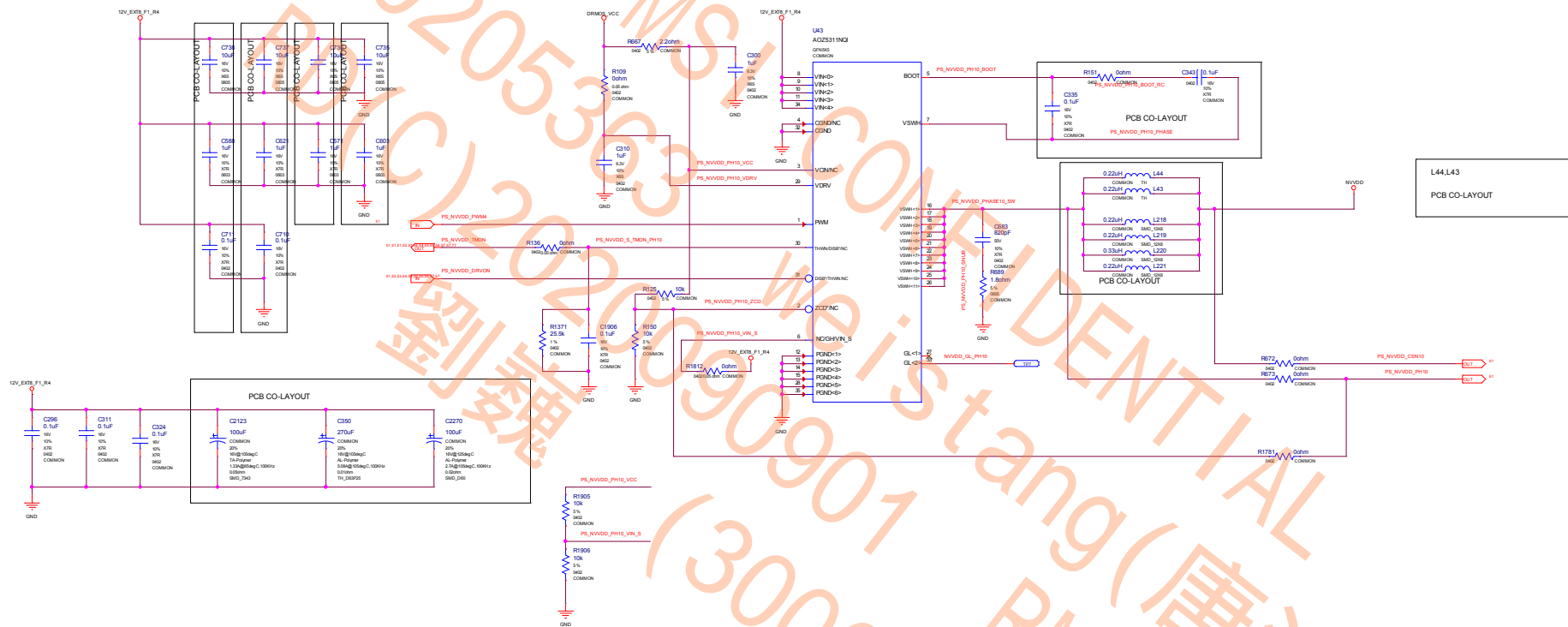
Size Custom	Document Description PS: NWDD PH 5, PH7	Rev 1.1
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PS: NVVDD Phase 6(PWM4)



PS: NVVDD PH 8 (PWM5), PH 9(PWM2)





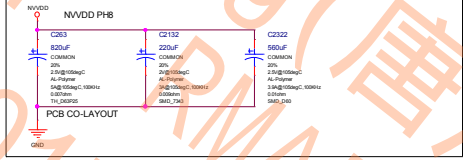
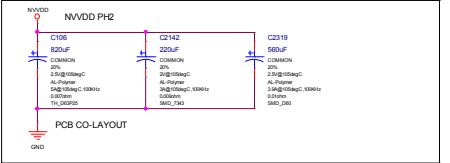
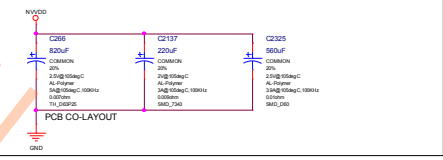
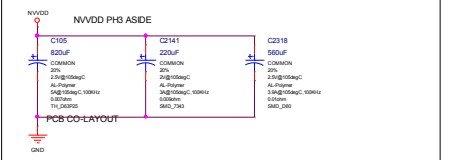
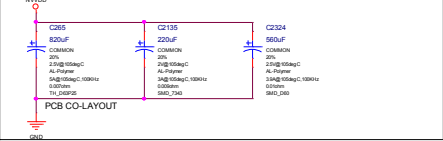
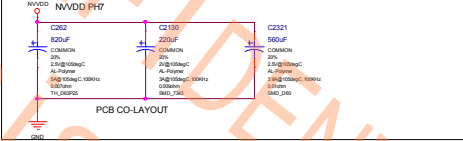
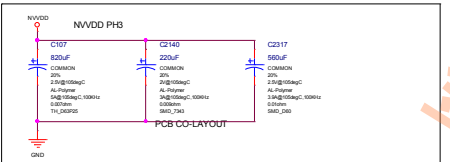
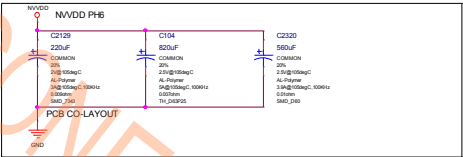
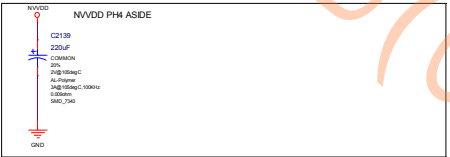
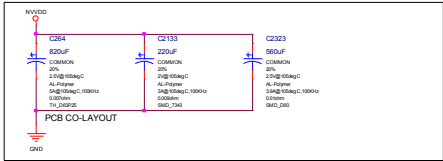
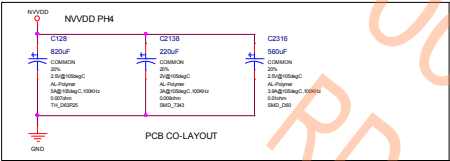
MSI CONFIDENTIAL
00205363
RD(C)2020090901
劉魏
weistang(唐浩健)
(30001789)
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MS-V388		
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REFER TO PCB FOR BOM STUFFING



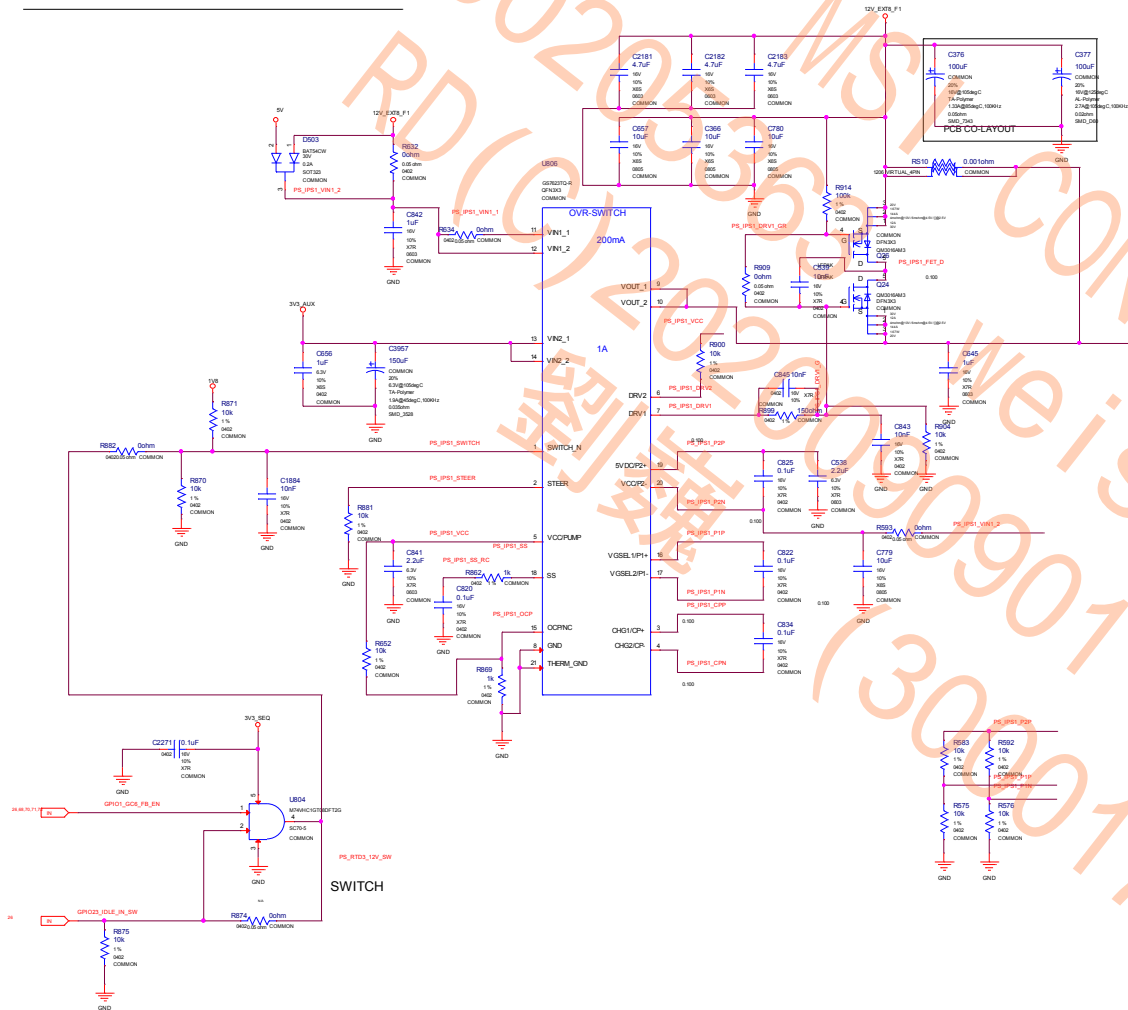
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			MICRO-STAR INT'L CO.,LTD	
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



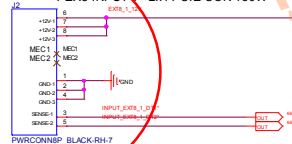
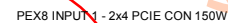
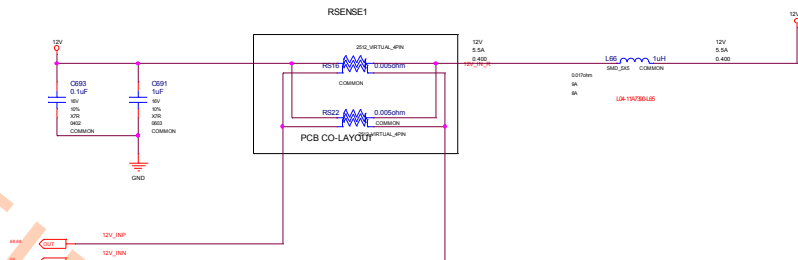
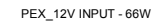
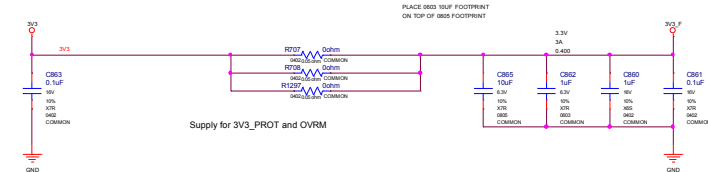
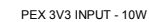
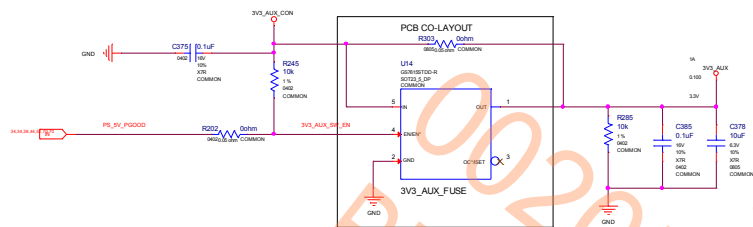
MICRO-STAR INT'L CO.,LTD
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Size Custom	Document Description PS: INPUT SWITCH RTD3	Rev 1.1
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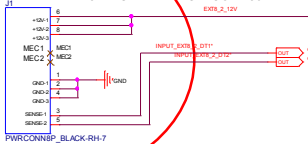
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MICRO-STAR INT'L CO.,LTD		
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Size	Document Description	Rev
Custom	BLANK	1.1
Date: Wednesday, July 22, 2020		Sheet 64 of 78

PS: Inputs, Filtering, and Monitoring

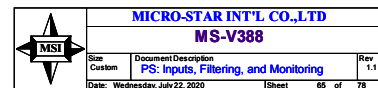
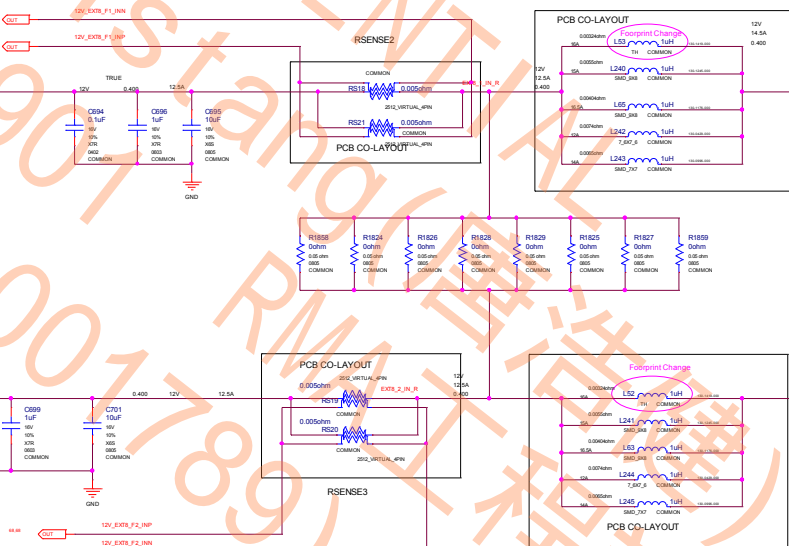


改反向8pin

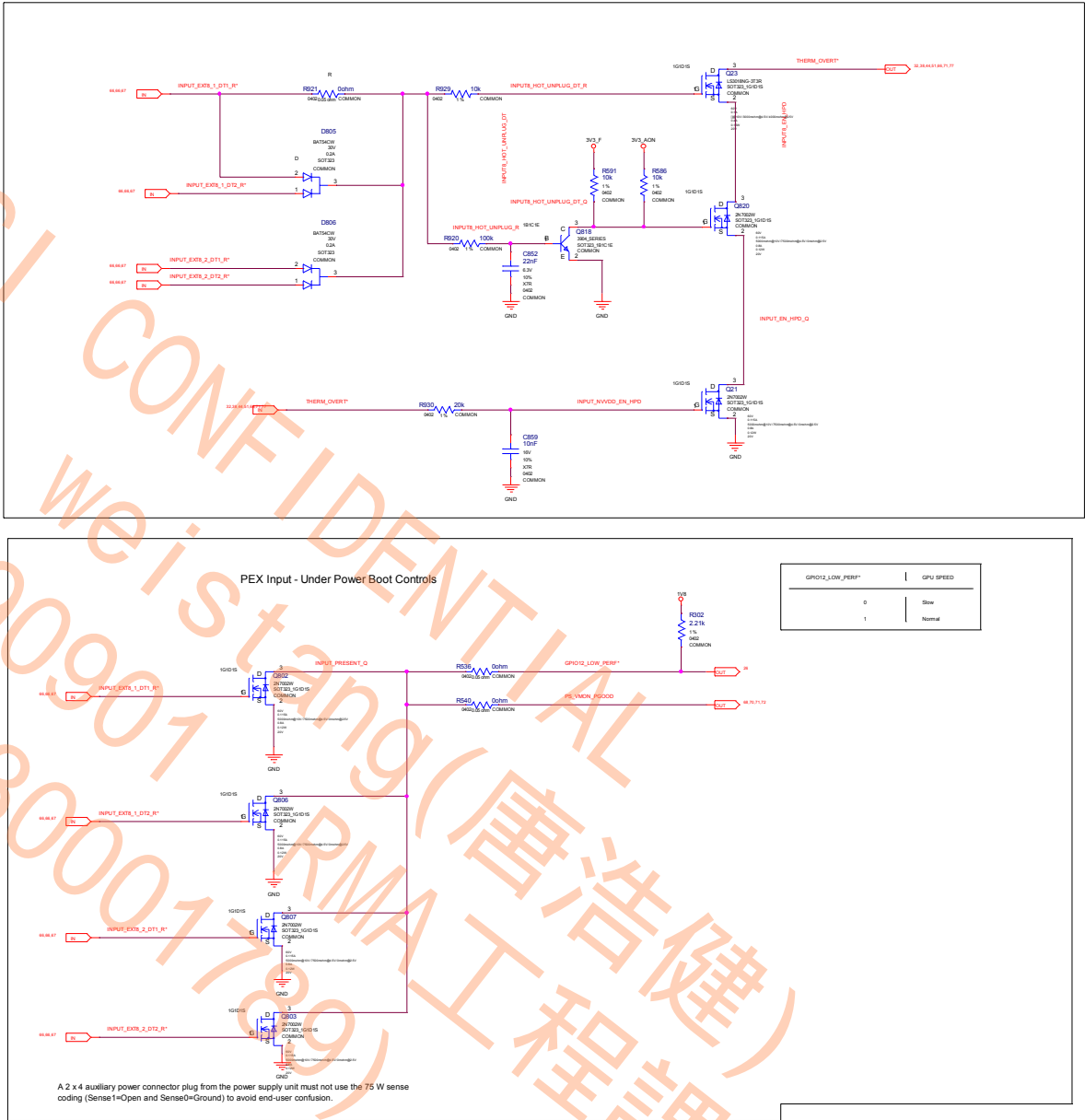
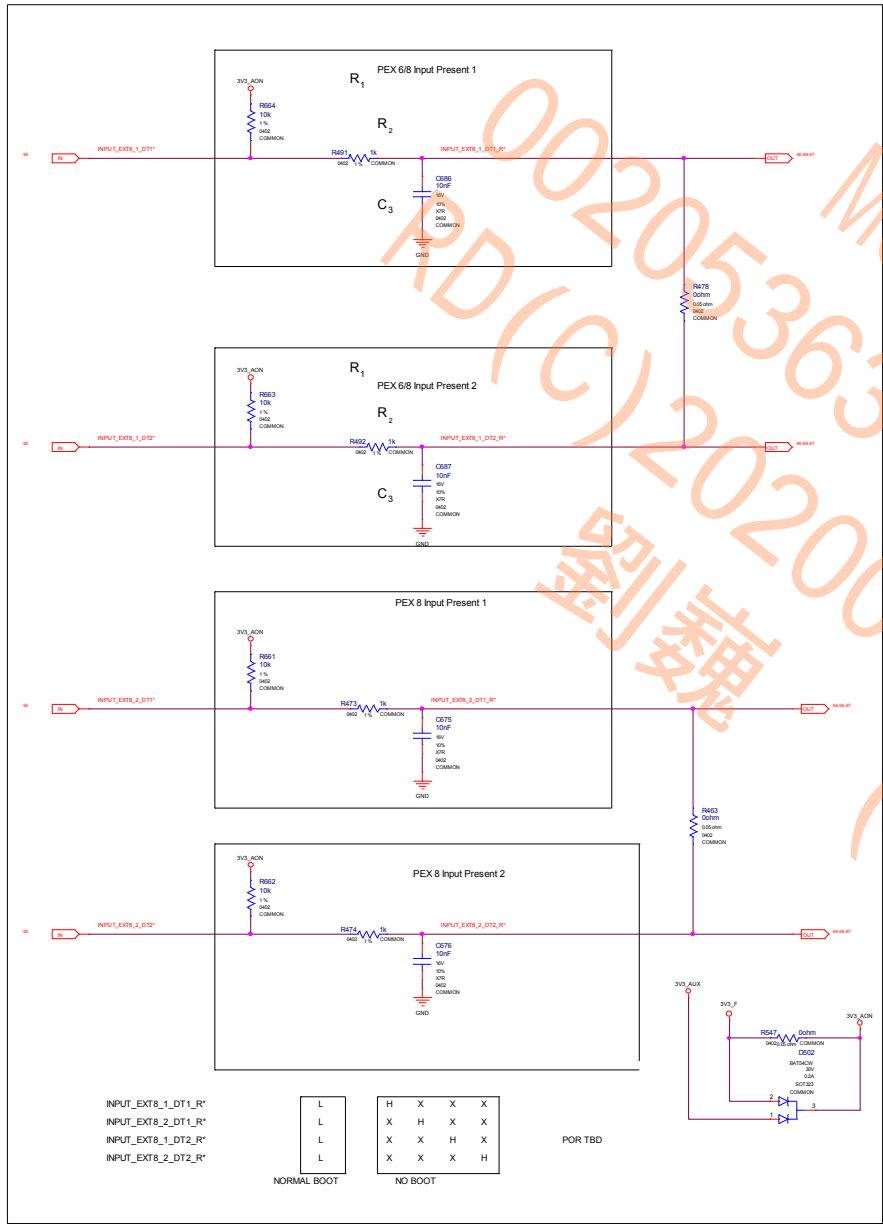


J24,J25,J26,J27 Remove

QD SKU CABLE



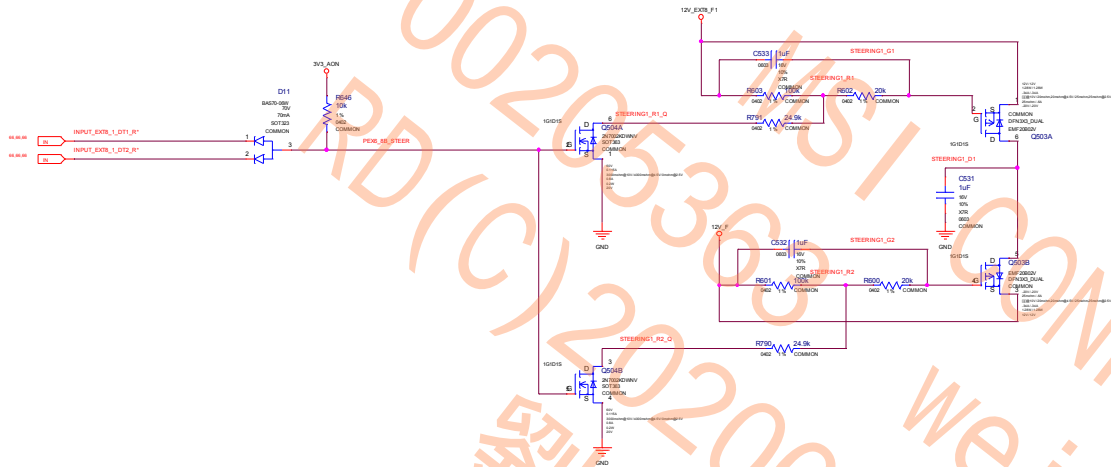
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

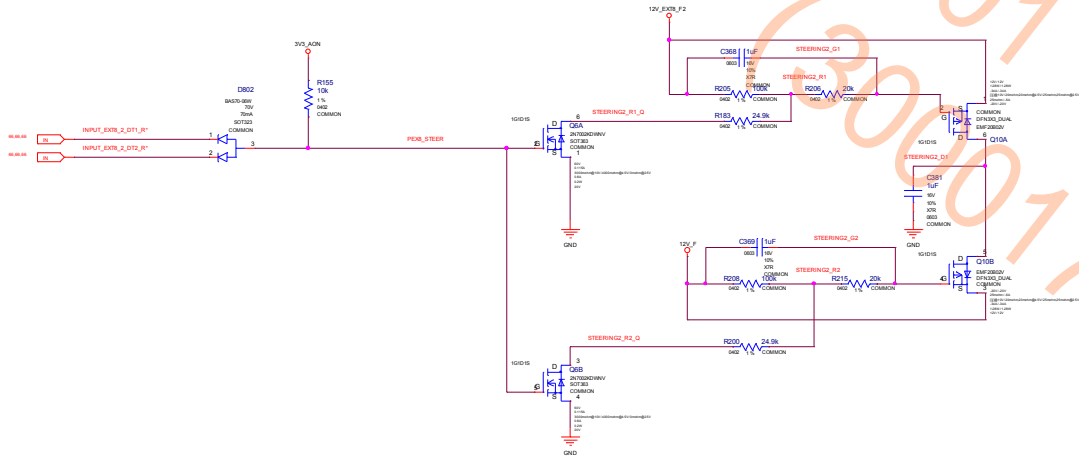
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



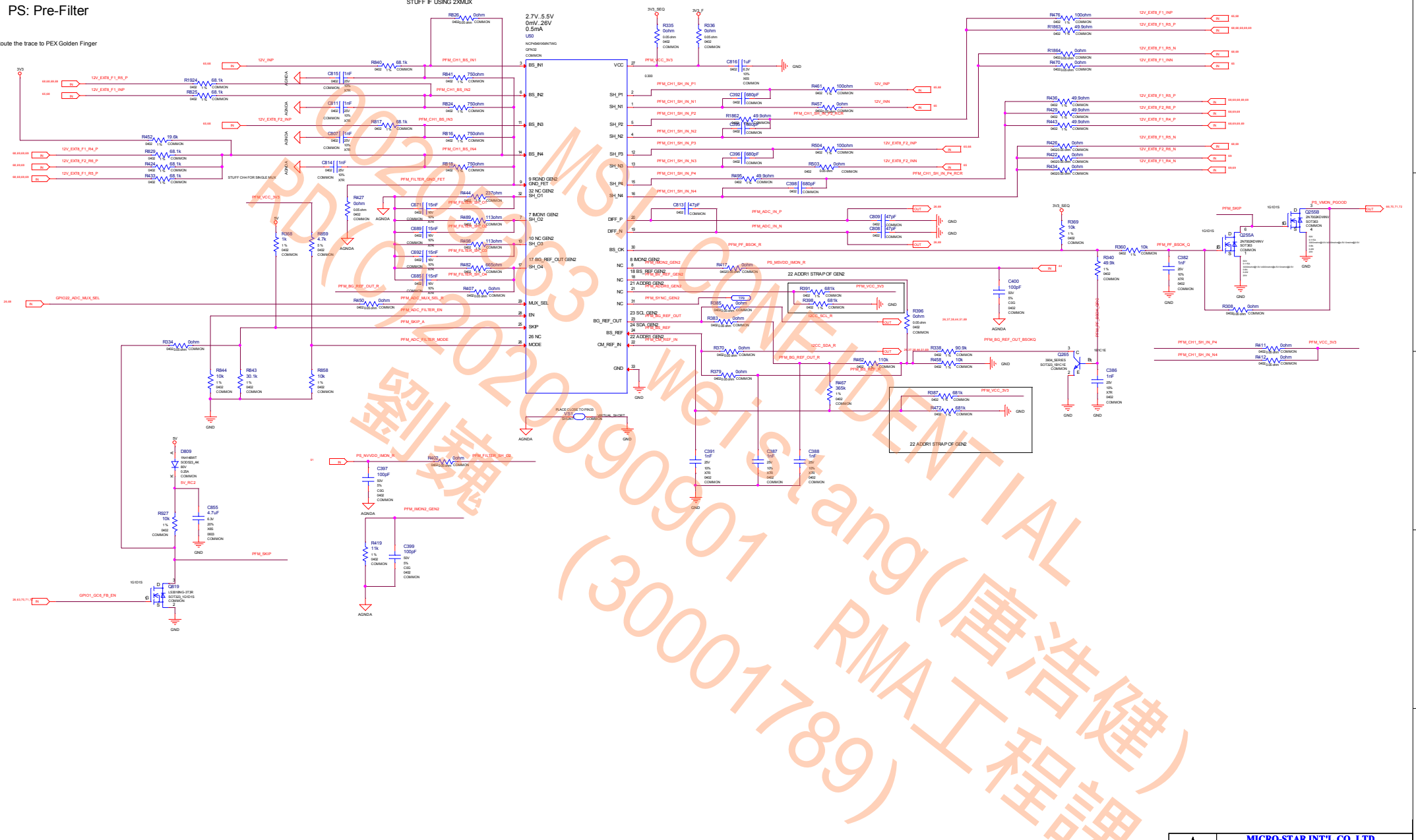
MICRO-STAR INT'L CO.,LTD		
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Size	Document Description	Rev
Custom	PS: Discrete Steering	1.1
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PS: Pre-Filter

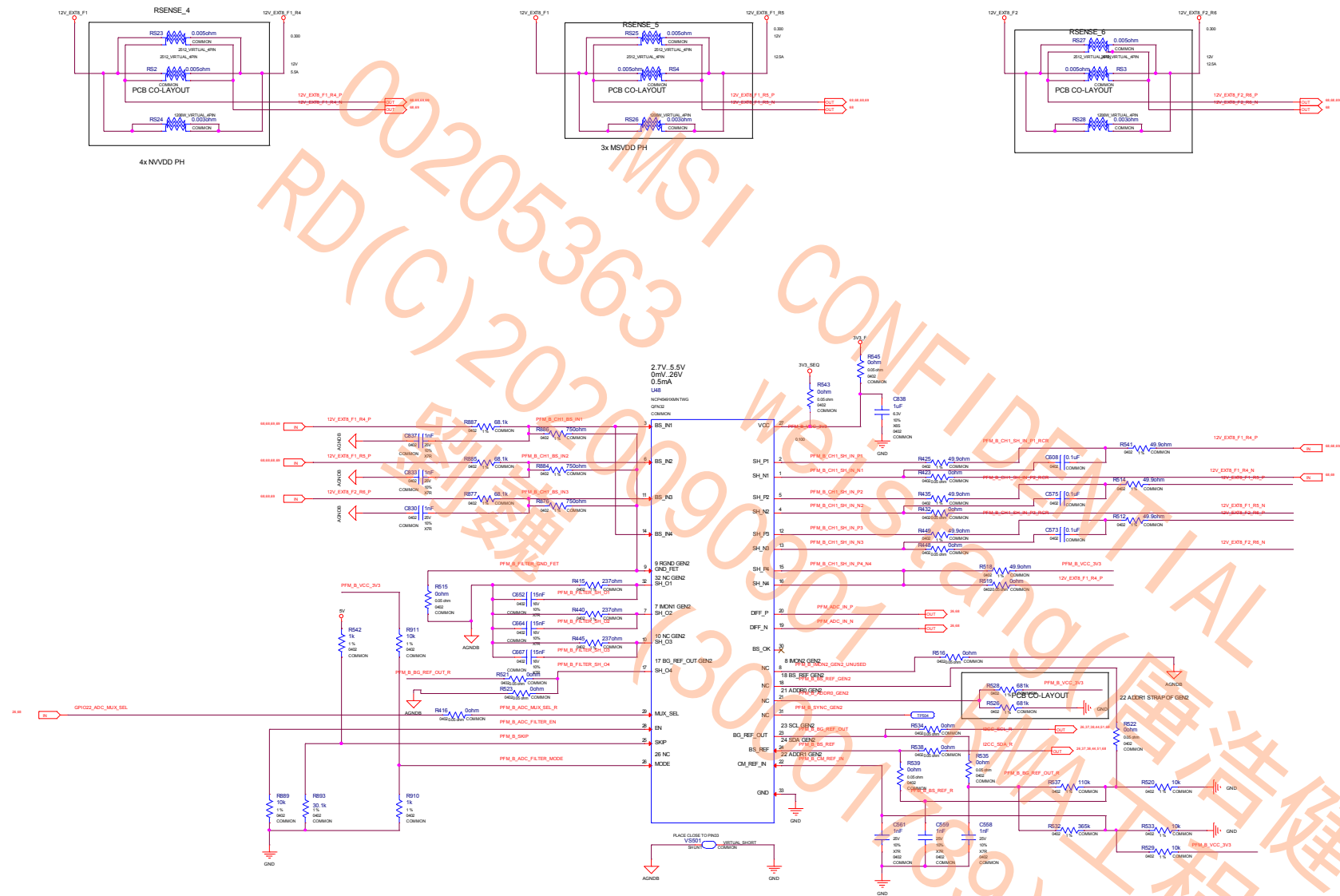
Route the trace to PEX Golden Finger

STUFF F USING 2XMUX

2.7V 5.5V
0mV 26V
0.5mA
NOISE/RESETTING
COMMON



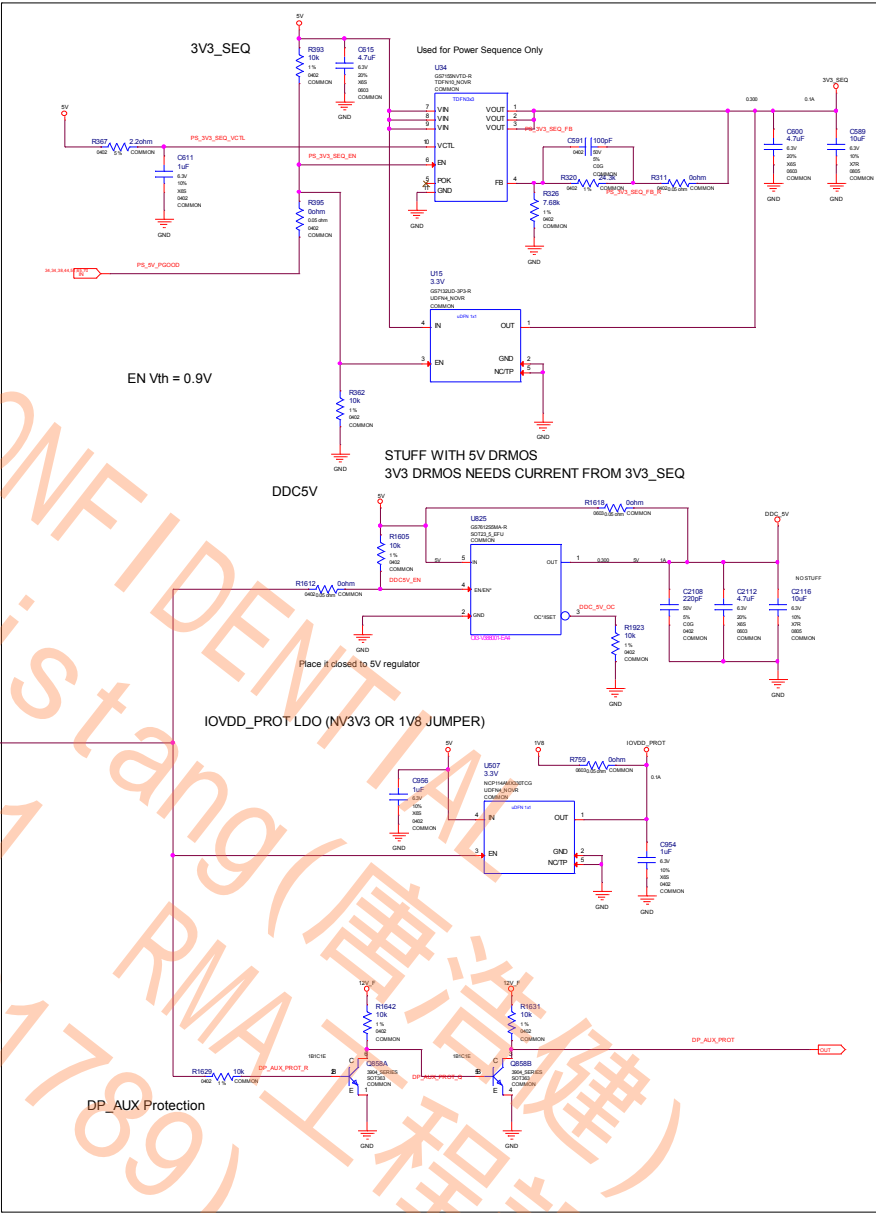
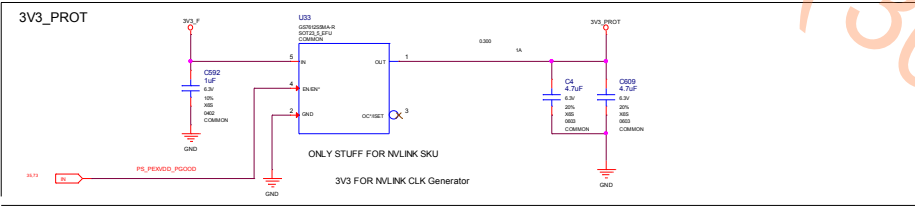
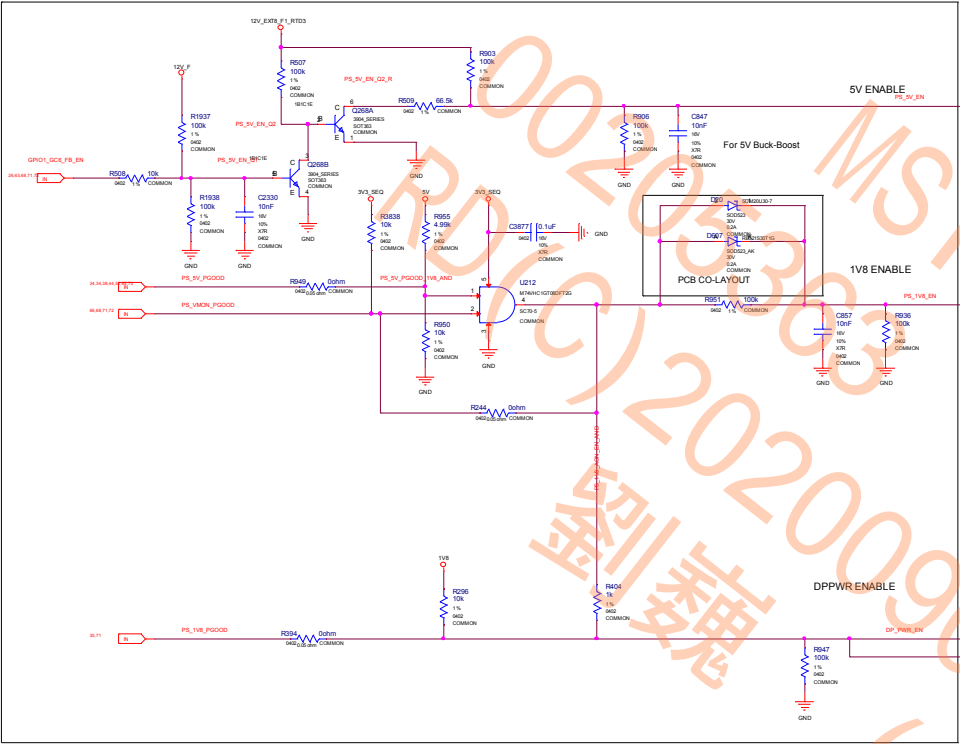
PS: Pre-Filter B

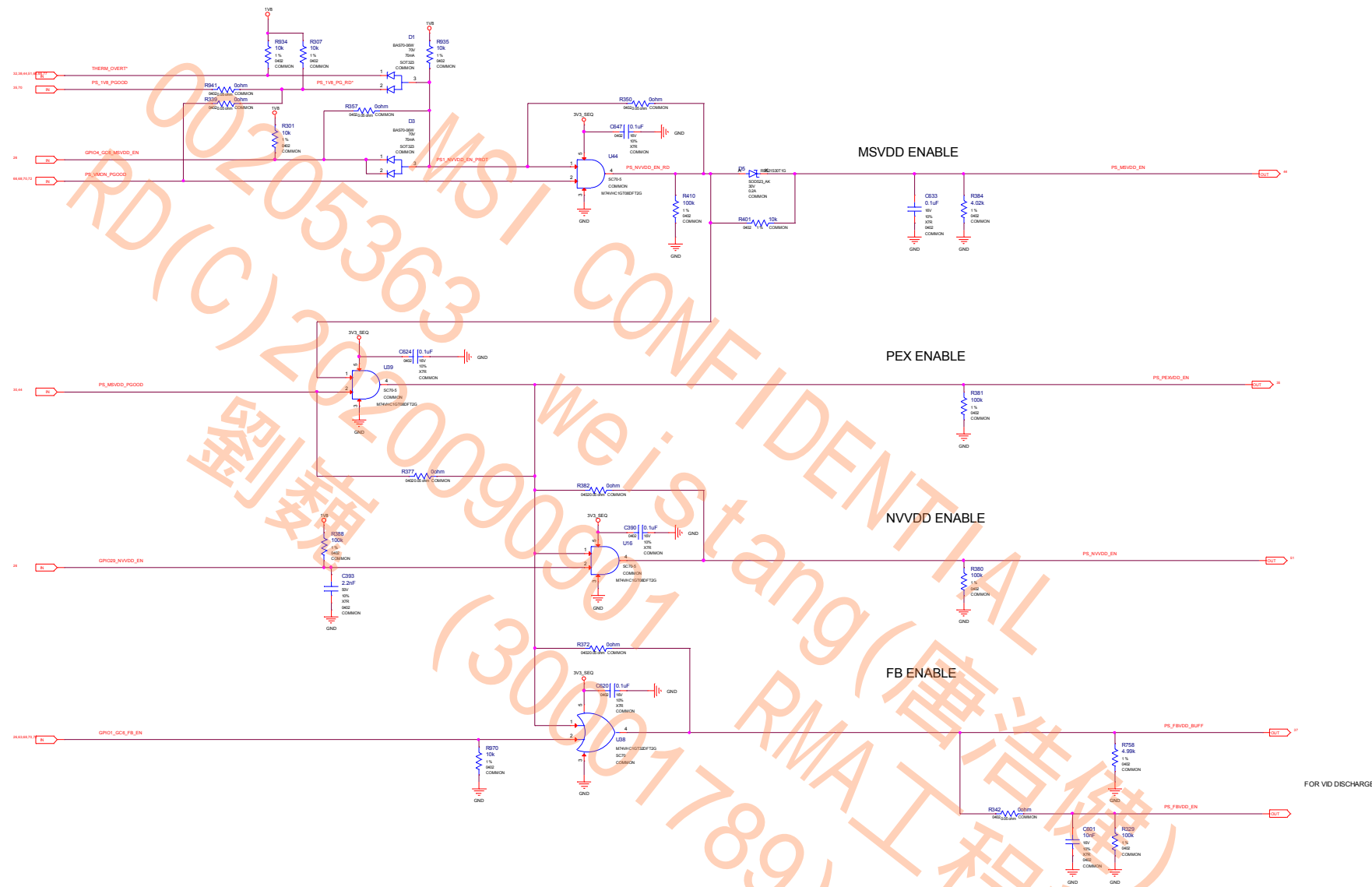


MICRO-STAR INT'L CO.,LTD
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Size Custom	Document Description PS: Pre-Filter B	Rev 1.
Date: Wednesday, July 22, 2020	Sheet	69 of 78

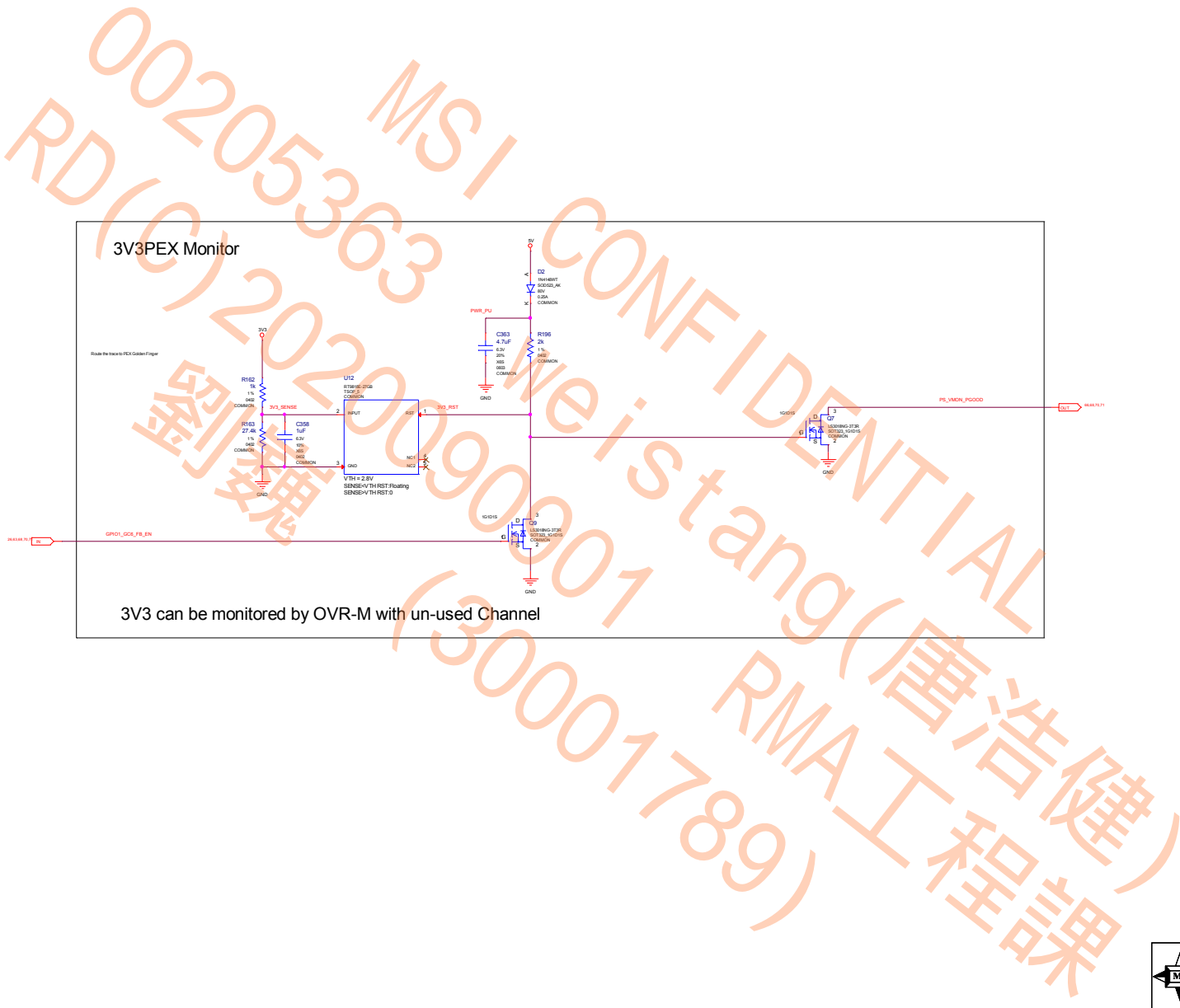
SEQUENCE:5V,1V8,3V3_SEQ ENABLE

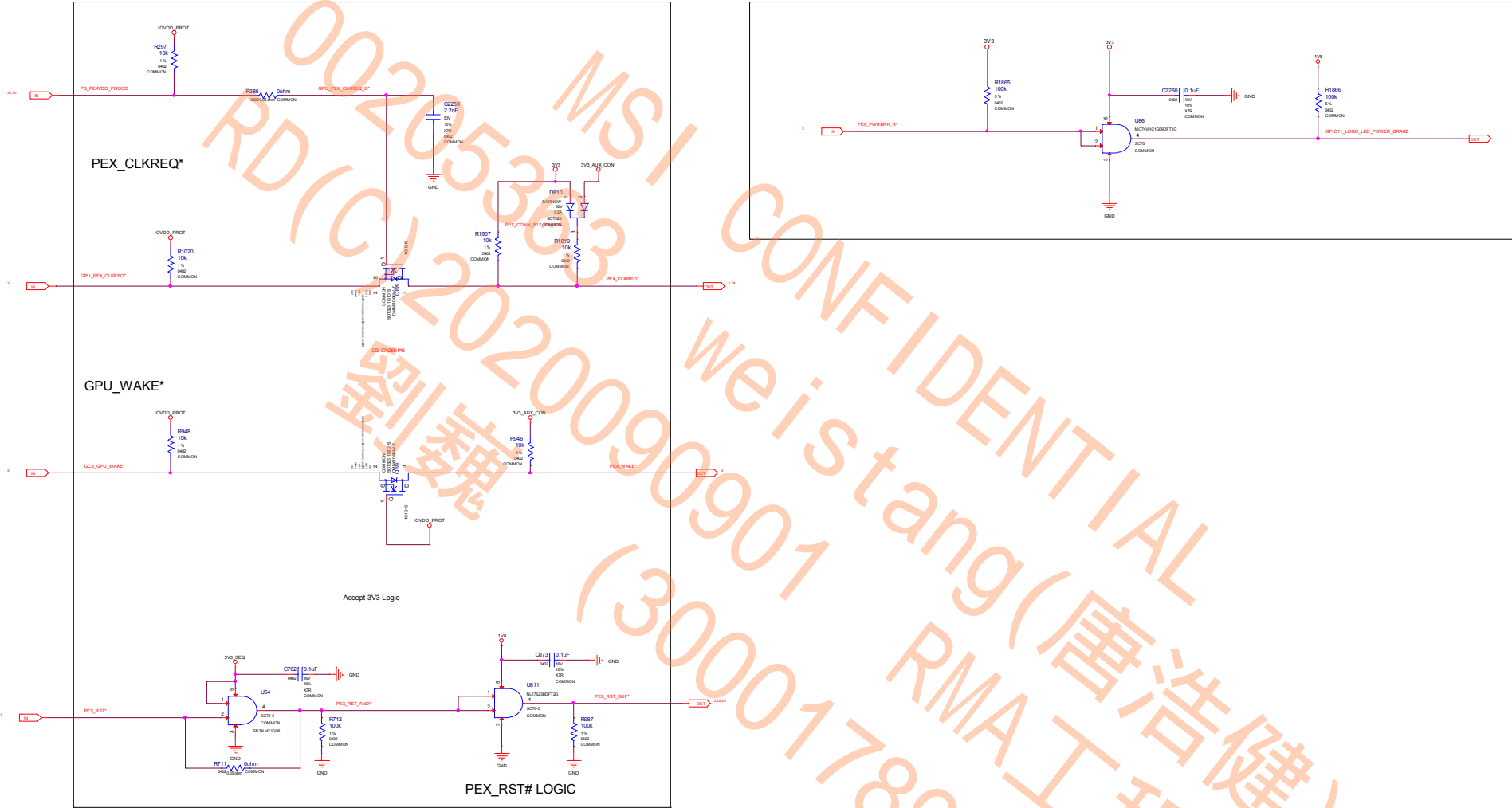




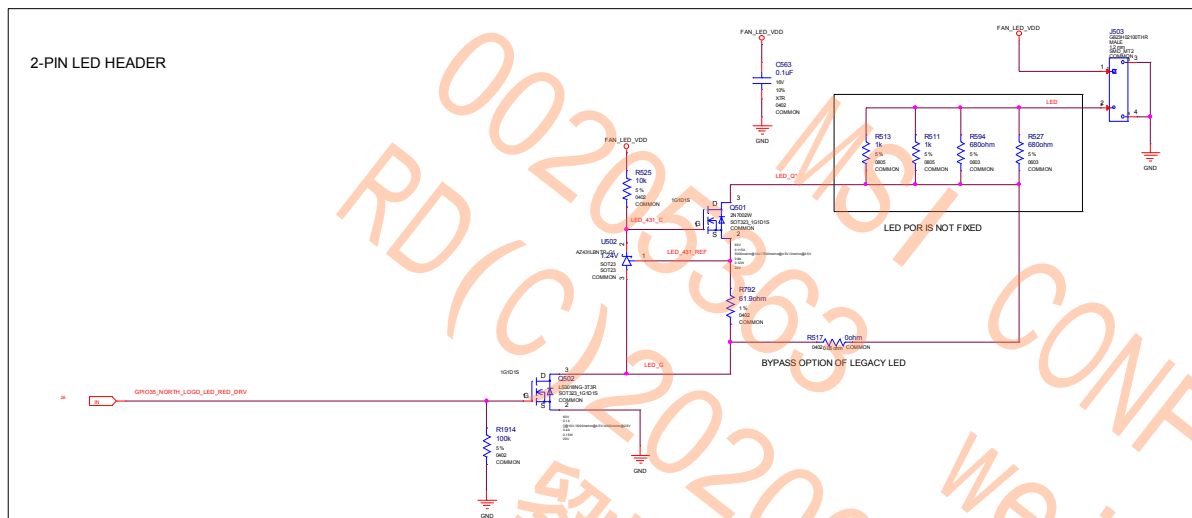
MICRO-STAR INT'L CO.,LTD
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Size Custom	Document Description SEQUENCE:NV,PEX,FB ENABLE	Re 1
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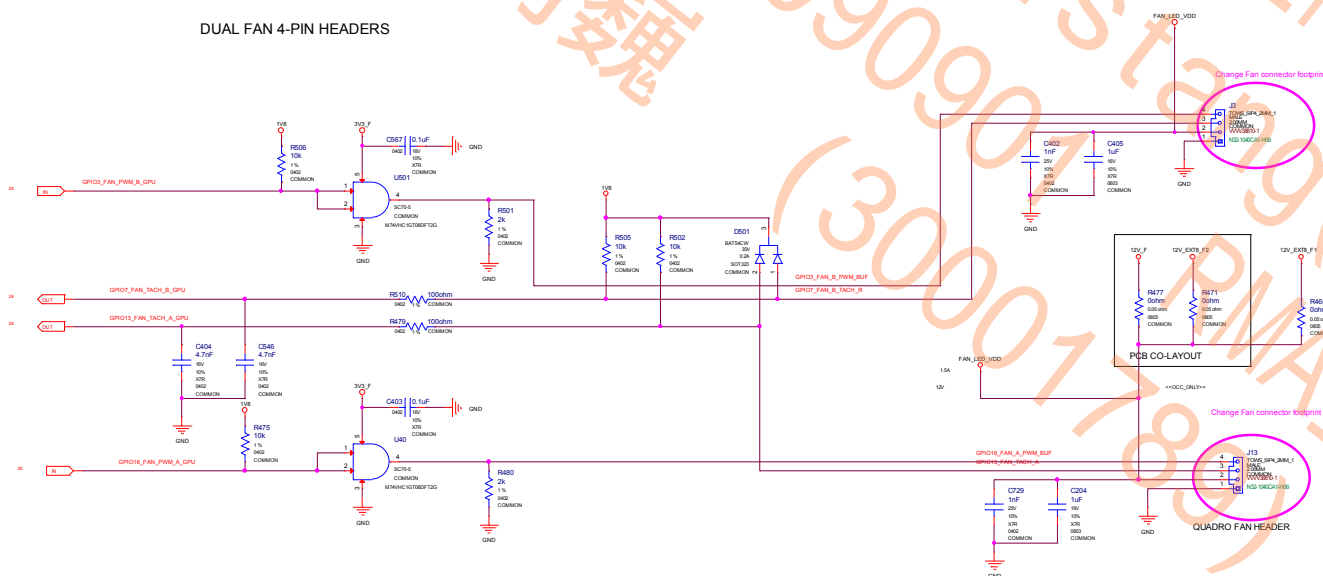




2-PIN LED HEADER

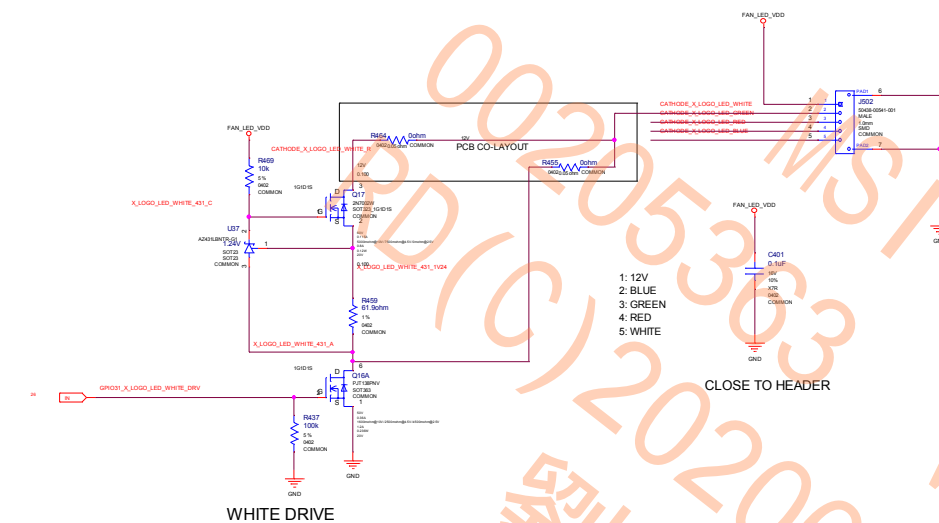


DUAL FAN 4-PIN HEADERS

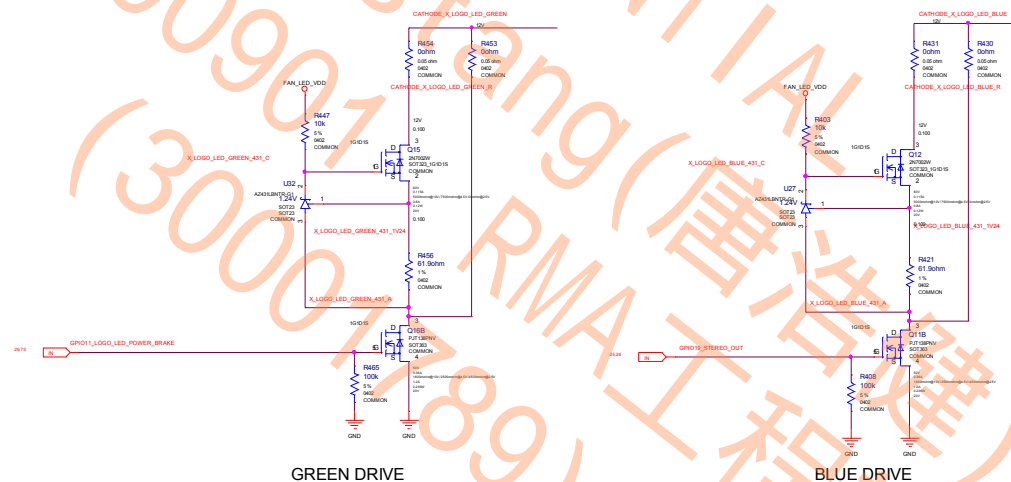
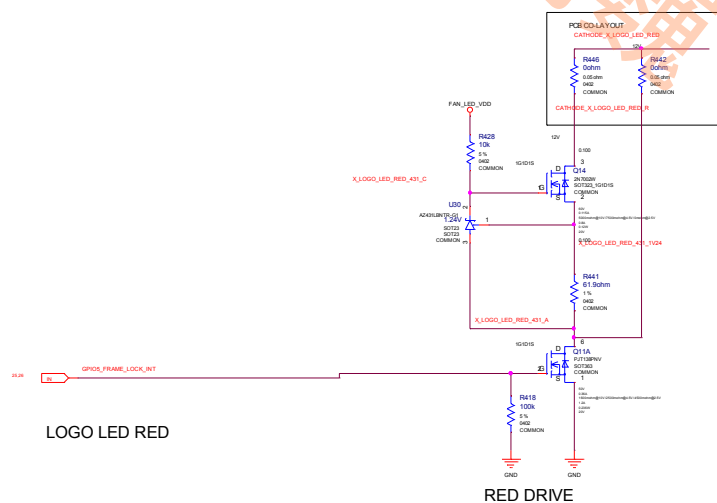


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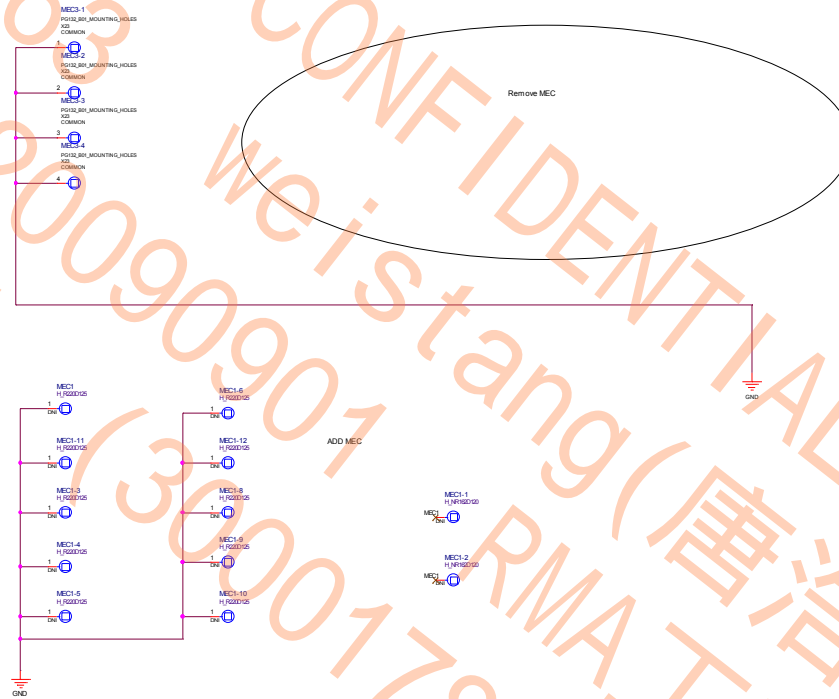
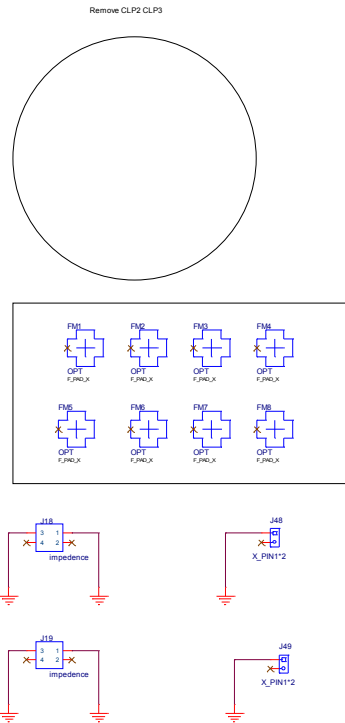
Size Custom	Document Description MISC: LED & FAN	Rev 1.
Date: Wednesday, July 22, 2020	Sheet	74 of 78



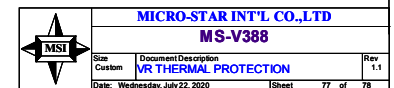
CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.



Mechanical: Mounting holes



VR THERMAL PROTECTION



PCI TERM

